



Universiti
Malaysia
PAHANG

Engineering • Technology • Creativity

FACULTY OF ELECTRICAL & ELECTRONICS ENGINEERING
FINAL EXAMINATION

COURSE	:	DIGITAL ELECTRONICS
COURSE CODE	:	BEE1213
LECTURER	:	FARADILA NAIM MARLINA YAKNO NURUL WAHIDAH ARSHAD
DATE	:	11 JANUARY 2016
DURATION	:	3 HOURS
SESSION/SEMESTER	:	SESSION 2015/2016 SEMESTER I
PROGRAMME CODE	:	BEE/BEP

INSTRUCTIONS TO CANDIDATES:

1. This question paper consists of **FIVE (5)** questions.
2. **ANSWER ONLY ONE** question in **PART A**. **ANSWER ALL** questions from **PART B**.
3. All answers to a new question should start on new page.
4. All calculations and assumptions must be clearly stated.
5. Question 2(a) and 3(b) must be answered in Appendix A and B. Attach the appendices to your answer booklet. Failure to submit the appendices along with your answer booklet before leaving the examination hall **WILL NOT BE ENTERTAINED**.

EXAMINATION REQUIREMENTS:

1. **Appendix A : Answer Sheet for Question 2(b)**
2. **Appendix B : Answer Sheet for Question 3(a)**

DO NOT TURN THIS PAGE UNTIL YOU ARE TOLD TO DO SO

This examination paper consists of **FOURTEEN (14)** printed pages including front page

PART A: ANSWER ONLY ONE QUESTION

QUESTION 1

(a) Perform the following operations.

- (i) Convert $ABCD_{16}$ to decimal
- (ii) Convert 205_{10} to binary
- (iii) Encode 187_{10} in BCD

[6 Marks]
[CO1, PO1, C2]

(b) Table 1 shows a voltage specification for two types of logic gates. Based on Figure 1 the input and output logic for gate any logic gates. Determine the following:

- (i) Is gate A specification valid for HIGH-state operation? Explain.
- (ii) Is gate B specification valid for LOW-state operation? Explain.

[4 Marks]
[CO1, PO1, C2]

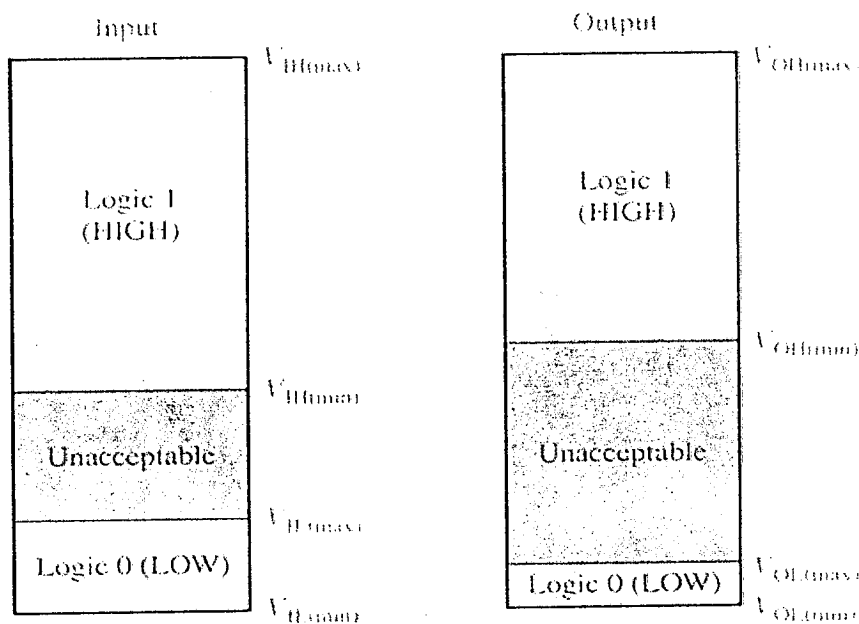


Figure 1

Table 1

	$V_{OH(MIN)}$	$V_{OL(MAX)}$	$V_{IH(MIN)}$	$V_{IL(MIN)}$
Gate A	2.2 V		2.5 V	
Gate B		0.45 V		0.75V

- (c) Figure 2 shows a combinational logic circuit.
- Write the expression for the output of X.
 - Use DeMorgan's theorems to simplify the acquired in (i).
 - Derive the complete truth table for expression X.
 - Given three input waveforms A, B and C as shown in Figure 3. Applied the combinational logic gates operation and draw the output waveform. Draw your answer in **APPENDIX A** and attach it to your answer booklet

[10 Marks]
[CO1, PO1, C3]

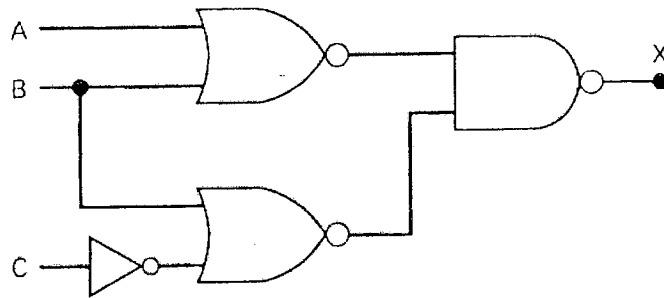


Figure 2

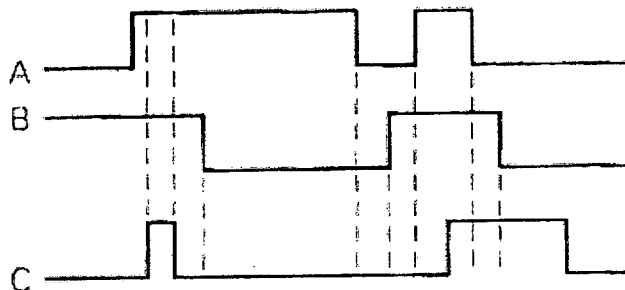


Figure 3

QUESTION 2

(a) Figure 4 shows a diagram for an automobile alarm circuit used to detect certain undesirable conditions. The three input switches are used to indicate the status of the door by the driver's seat, the ignition, and the headlights, respectively. The alarm will be activated when either of the following conditions is met:

- The headlights are on while the ignition is off.
- The door is open while the ignition is on.

- (i) Derive the truth table and SOP expression for the system.
- (ii) Use algebraic simplification to simplify the SOP expression acquired in (i).
- (iii) Prove your simplified expression using K-maps.
- (iv) Implement the simplified expression into logic circuit diagram.

[10 Marks]
[CO1, PO1, C3]

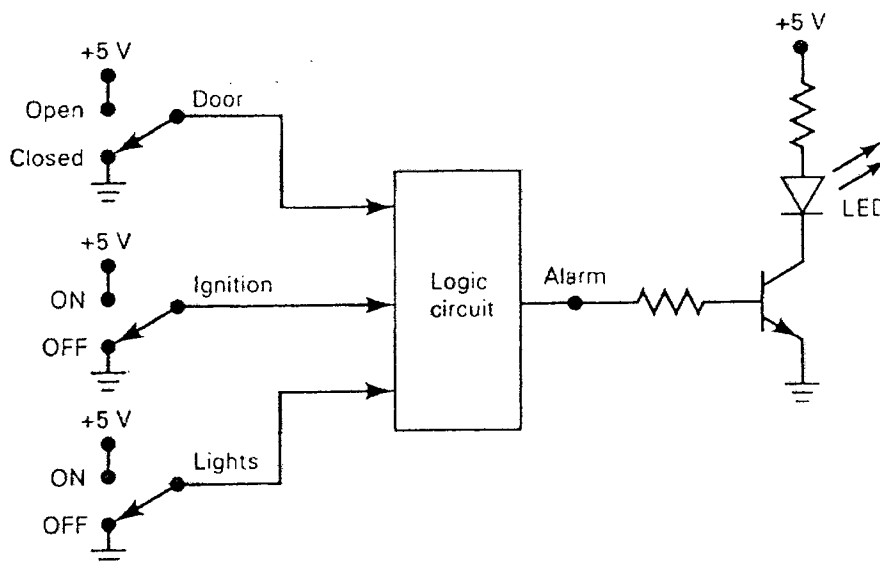


Figure 4

(b) Given two signed binary number, $A = 0000\ 1110$ and $B = 1110\ 1111$. Perform the following operations.

- (i) Addition ($A + B$)
- (ii) Subtraction ($A - B$)

[4 Marks]
[CO1, PO1, C2]

(c) A few sets of data from Table 2 and Table 3 are used to implement into the parity generator and parity checker for an **odd-parity system**. Use these values to determine the following:

- (i) The parity generator's output (P) for each of the following sets of data in Table 2.
- (ii) The parity checker's output (E) for each of the following sets of data in Table 3.

[6 Marks]
[CO1, PO1, C3]

Table 2

P	D3	D2	D1	D1
	0	1	1	1
	1	0	0	1
	0	1	0	0

Table 3

P	D3	D2	D1	D1	E
1	0	1	1	1	
1	1	0	0	1	
1	0	1	0	0	

PART B: ANSWER ALL QUESTIONS

QUESTION 3

(a) The waveform shown in Figure 5 are to be applied to two different FFs:

- (i) Positive edge triggered J-K
- (ii) Negative edge triggered J-K

Draw the Q waveform response for each of these FFs, assuming that Q initially HIGH. Draw your answer in **APPENDIX B** and attach it to your answer booklet.

[9 Marks]
[CO2, PO2, C3]

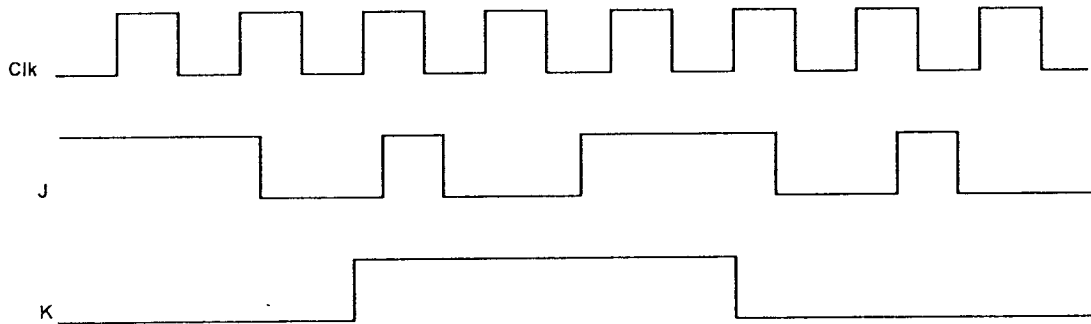


Figure 5

(b) Analyze the synchronous counter in Figure 6. Draw its timing diagram until 10th clock pulse and determine the counter's modulus. Given the input clock frequency is 10kHz.

[8 Marks]
[CO3, PO2, C3]

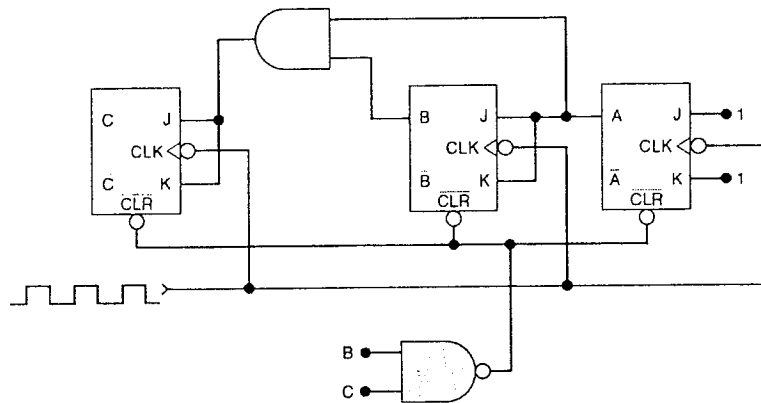


Figure 6

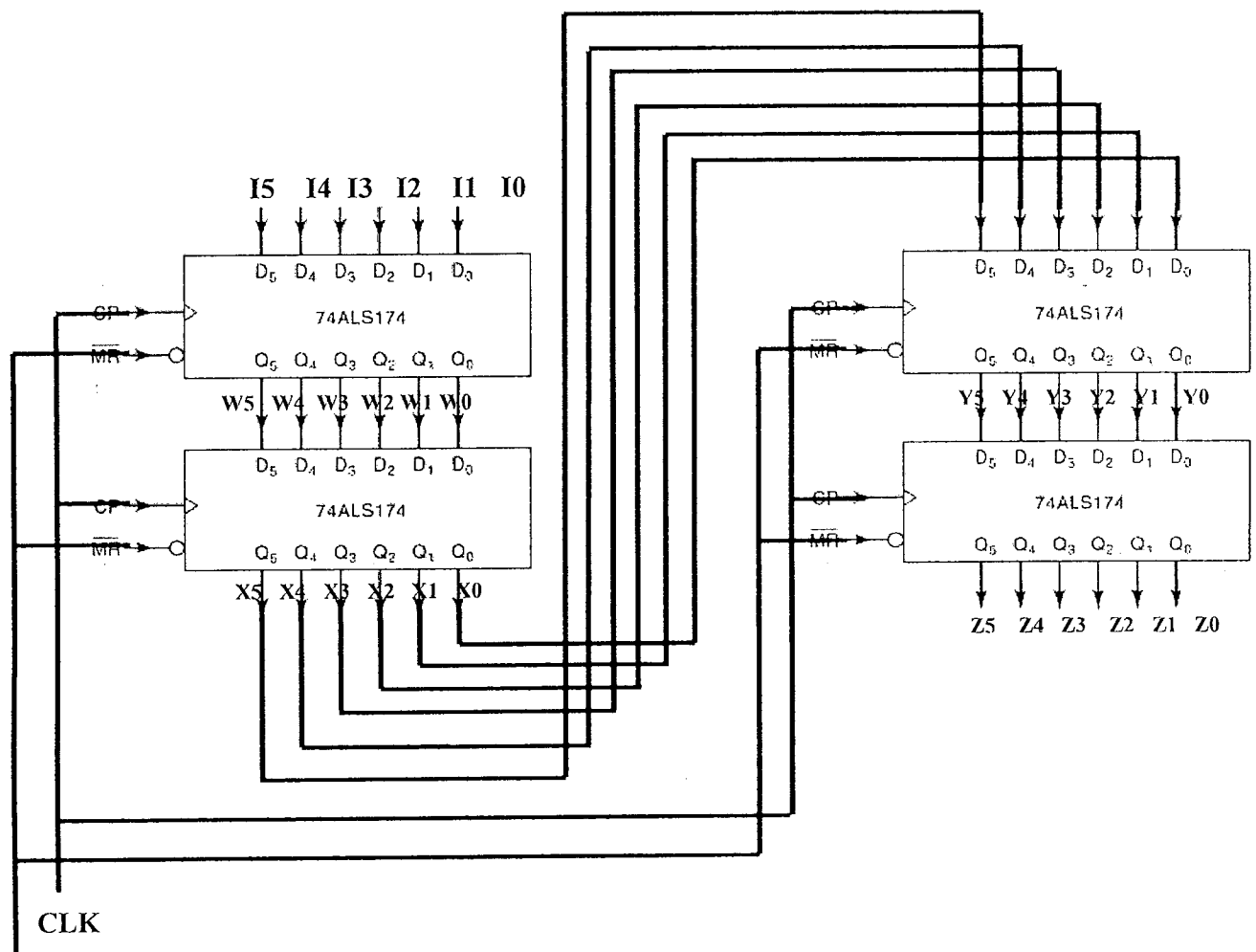
(c) Design the synchronous counter using J-K FFs that has the following sequence: 000, 010, 100, 110, and repeat. The undesired (unused) states must always go to 000 on the next clock pulse.

[13 Marks]
[C02, PO2,C3]

QUESTION 4

- (a) Figure 7 shown a set of 74ALS174 shift registers. \overline{MR} is a master reset input, can be used to reset asynchronously all of the register FFs to 0.
- (i) What type of data transfer is performed with each register?
 - (ii) Determine the output of each register when the \overline{MR} is pulsed momentarily LOW and after each of the indicated clock pulses (CP#) in Table 3.
 - (iii) How many clock pulses must be applied before data that are input on I5-I0 are available at Z5-Z0?

[13 Marks]
[CO2, PO2, C4]



\overline{MR}

Figure 7

Table 3

\uparrow CLK	\overline{MR}	I5-I0	W5-W0	X5-X0	Y5-Y0	Z5-Z0
X	0	101111				
CP1	1	101111				
CP2	1	000011				
CP3	1	101010				
CP4	1	110000				
CP5	1	011000				
CP6	1	111000				
CP7	1	000000				
CP8	1	000000				

(b) For each statement below, indicate whether it is referring to a decoder, an encoder, a MUX, or a DEMUX (only write your answer in answer sheet) ;

- (i) Has more inputs than outputs.
- (ii) Uses SELECT inputs
- (iii) Can be used in parallel-to-serial conversion.
- (iv) Only one of its outputs can be activate at one time.
- (v) Can be used to route an input signal to one of several possible outputs.

[5 Marks]
[CO2, PO2, C2]

- (d) Given in Figure 8 is the logic symbol for 4-bit full adder.
- (i) Design the 4-bit full adder using four full-adder.
 - (ii) Perform the binary addition of $A = 1010$ and $B = 0011$.

[12 Marks]
[CO2, PO2, C3]

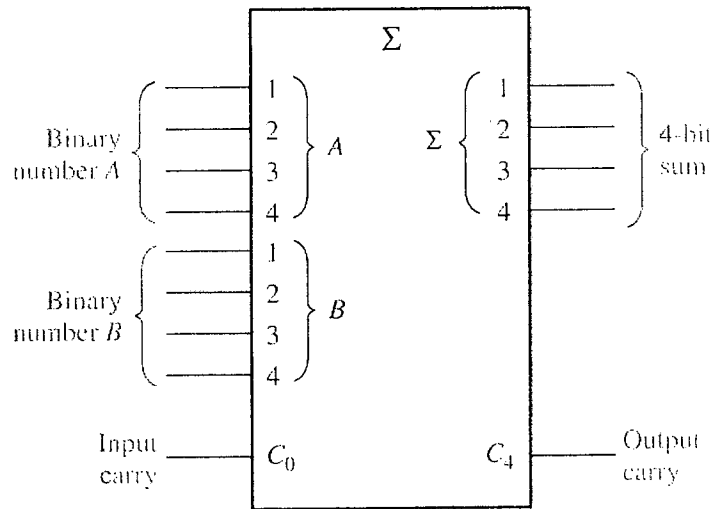


Figure 8

QUESTION 5

(a) EEPROM is an Electrically Erasable Programmable ROM. Figure 9 is the symbol for a 16K x 16 EEPROM. Answer the following questions.

[14 Marks]
[CO3, PO1, C4]

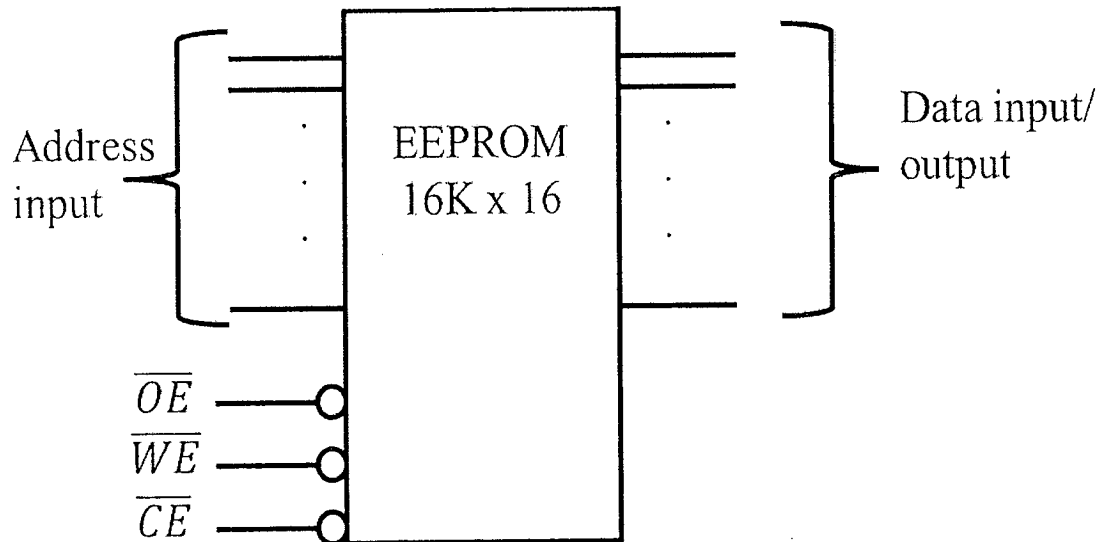


Figure 9

- (i) How many words does it store?
- (ii) What is the number of bits per word?
- (iii) How many rows and columns does it have?
- (iv) How many address lines does it have?
- (v) How many data input and data output lines does it have?
- (vi) How many total bits can this chip store?
- (vii) What is its capacity on bytes?
- (viii) Gives the input combinations for \overline{OE} , \overline{CE} and \overline{WE} , in write mode and read mode.

(b) For each item below, indicate the type of memory being described: PROM, EPROM, and EEPROM. Some items will correspond to more than one memory type

[6 Marks]
[CO3, PO1, C3]

- (i) Can be programmed once.
- (ii) Is erased electrically
- (iii) Once programmed, it cannot be reversed.
- (iv) Erase time is about 15 to 20 minutes
- (v) Is erased with UV light
- (vi) Uses fusible links

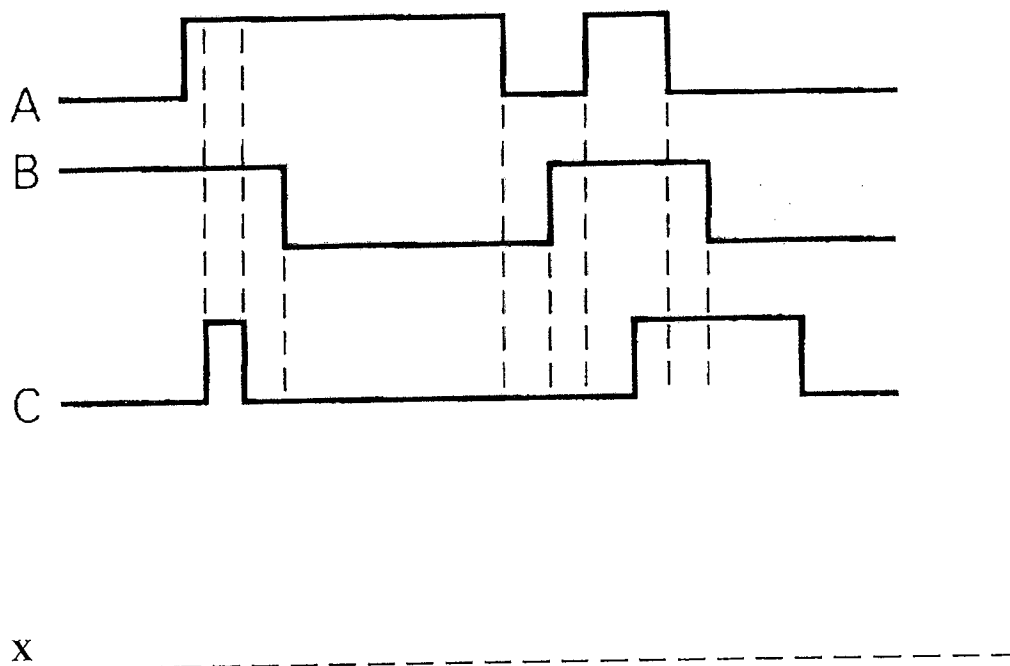
END OF QUESTION PAPER

APPENDIX A

Time waveform for question 1(c)

ID : _____

IC : _____

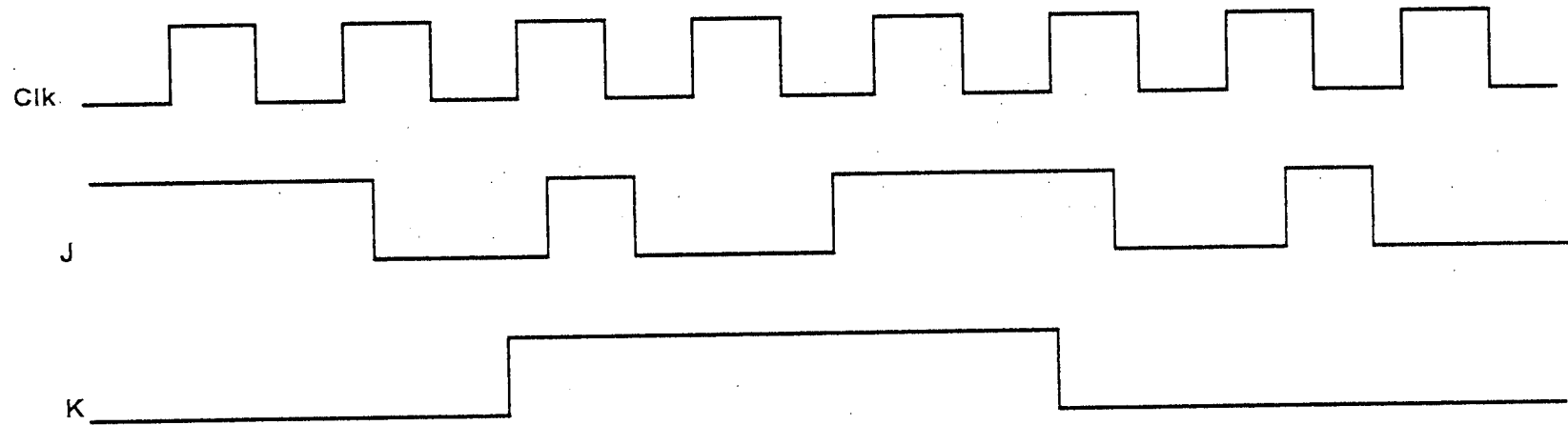


APPENDIX B

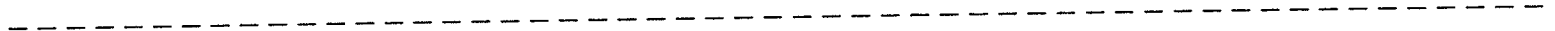
Time waveform for question 3(a)

ID : _____

IC : _____



(i) Q for PGT



(ii) Q for NGT

