Universiti Malaysia PAHANG

Engineering • Technology • Creativity

FACULTY OF ELECTRICAL & ELECTRONICS ENGINEERING

FINAL EXAMINATION

COURSE	:	**DIGITAL ELECTRONICS**
COURSE CODE	:	**BEE1213**
LECTURER	:	**FARADILA NAIM** **NURUL WAHIDAH ARSHAD**
DATE	:	**7 JANUARY 2015**
DURATION	:	**3 HOURS**
SESSION/SEMESTER	:	**SESSION 2014/2015 SEMESTER I**
PROGRAMME CODE	:	**BEC/BEE/BEP**

INSTRUCTIONS TO CANDIDATES

1. This question paper consists of **FIVE (5)** questions. **ANSWER ALL** questions from **PART A** and **ONLY ONE** questions in **PART B**.
2. All answers to a new question should start on new page.
3. All the calculations and assumptions must be clearly stated.
4. Question 2(a) must be answered in Appendix A, attach to your answer sheet. Failure to submit the appendix along with your answer booklet before leaving the examination hall **WILL NOT BE ENTERTAINED.**

EXAMINATION REQUIREMENTS

1. **Appendix A: Timing Diagram for question 2(a).**

DO NOT TURN THIS PAGE UNTIL YOU ARE TOLD TO DO SO

This examination paper consists of **TWELVE (12)** printed pages including front page

PART A: ANSWER ALL QUESTIONS

QUESTION 1

(a) Determine the weight of the 1 in the binary number 001000.

[2 Marks]
[CO1, PO1, C2]

(b) Convert the binary number 11.001 to decimal number.

[2 Marks]
[CO1, PO1, C2]

(c) Given 2 binary number, A=1100 and B=10. Perform the following operations:

(i) Addition (A+B)

(ii) Subtraction (A-B)

(iii)Multiplication (A×B)

(iv)Division (A÷B)

(v) Signed number subtraction (A-B)

[11 Marks]
[CO1, PO1, C2]

(d) Given a decimal number 999. Perform the following operations:

(i) Convert to hexadecimal.

(ii) Convert to BCD number

[5 Marks]
[CO1, PO1, C2]

QUESTION 2

(a) Given two input waveforms S and T as shown in Figure 1. Applied the basic logic gates operation and draw the output waveform. Draw your answer in **APPENDIX A** and attach with your answer booklet.

i) S OR T

ii) S AND B

iii) S XOR B

iv) A NAND B

[8 Marks]
[CO2, PO1, C2]

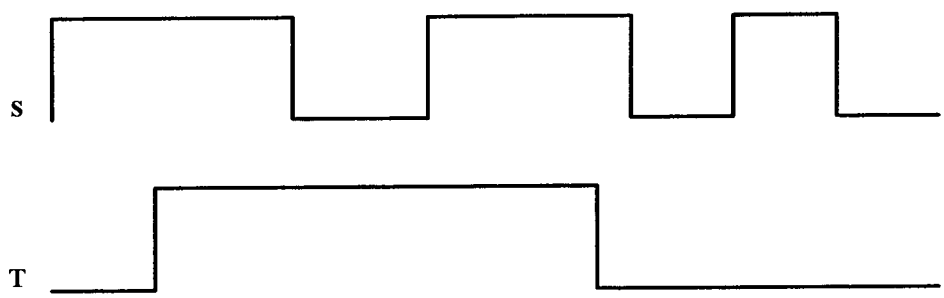


Figure 1

(b) Draw the circuit and truth table of intrusion detection system for one room in a home by using basic logic gate. The inputs of this system are two windows and a door. When one of the windows or the door is opened, a HIGH output is produced and activates the alarm circuit to warn of the intrusion.

[5 Marks]
[CO2, PO1, C3]

(c) Given a function $X = \overline{A} + A\overline{C} + AB\overline{C}$

(i) Simplify using Boolean algebraic

(ii) Simplify using Karnaugh Map

(iii)Implement the simplified expression from ii).

[9 Marks]
[CO2, PO1, C3]

(d) Segment *b* in 7-segment digit as illustrated in Figure 2 will be activated for the digits 0, 1, 2, 3, 4, 7, 8 and 9. Derive an SOP expression for segment b using the variables ABCD and minimize the expression using Karnaugh map. (Hint: Represent each digit by using BCD code)

[8 Marks]
[CO2, PO1, C3]

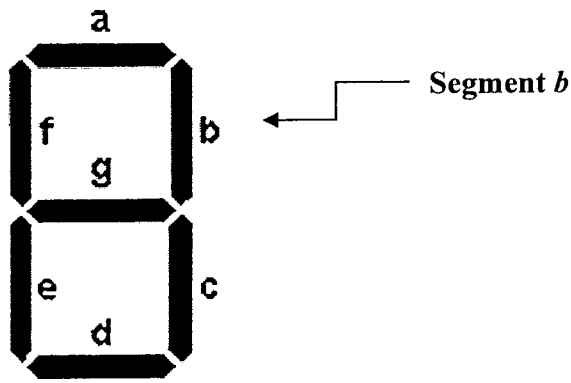
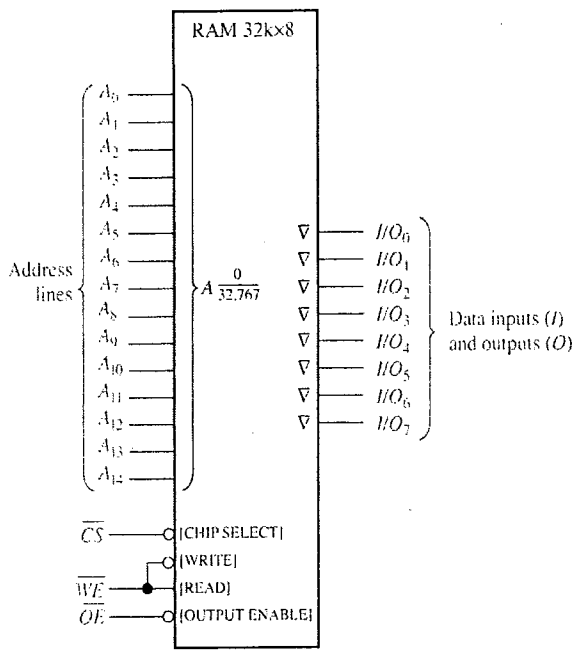


Figure 2

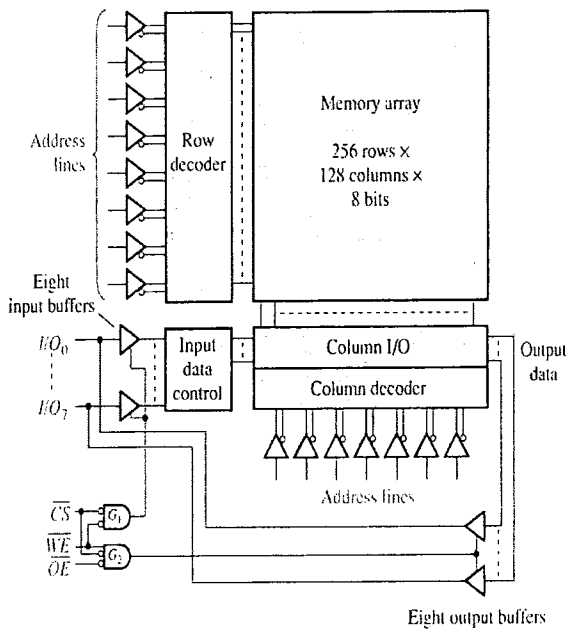
QUESTION 3

(a) RAM or *Random Access Memory* is a type of memory that can be accessed randomly. Given in Figure 3 is the information from a data sheet of a 32k × 8 RAM which include; (a) memory symbol, (b) internal architecture of the memory, (c) the timing waveform for read operation, and (d) the timing waveform for write operation . Fill in the blanks of the statements based on the information given in Figure 3. (Question with *[(ii) &(iii)], choose ONE answer from the statement inside bracket).

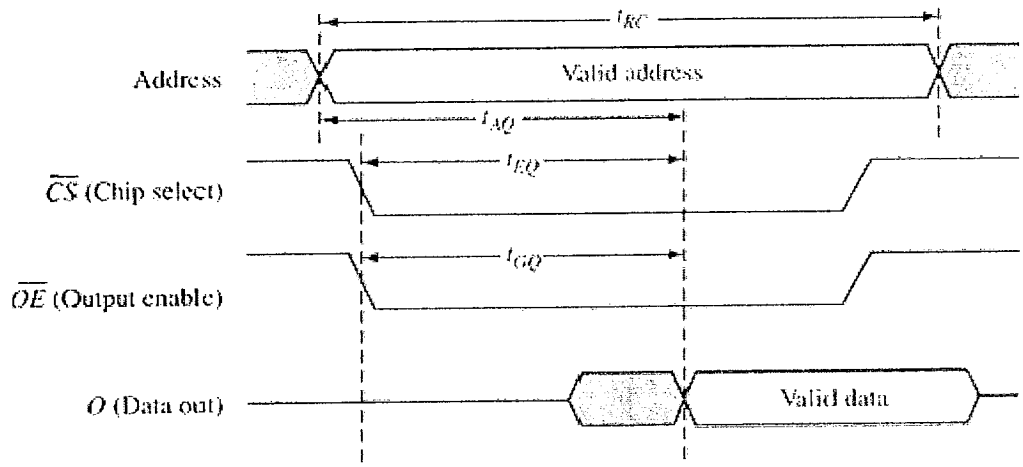
[15 Marks]
[CO3, PO1, C3]



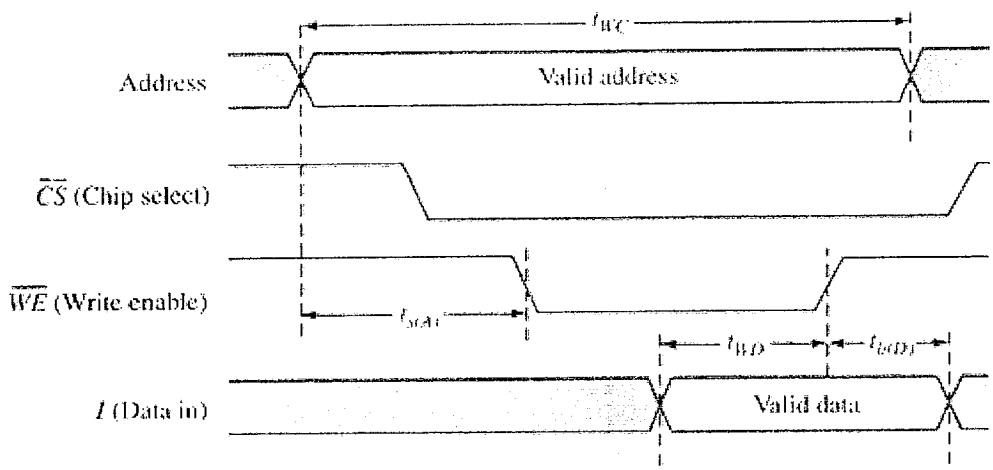
(a) Memory Symbol



(b) Internal Architecture



(c) Read Cycle Timing Waveform



(d) Write Cycle Timing Waveform

Figure 3

(i) RAM 32K x 8 has _____ memory locations with _____ data bits at each location.

(ii) RAM 32K x 8 has _____bits address input and _____ bits data output.

(iii) In read operation, $\overline{WE}$ must be ____ (HIGH /LOW) and $\overline{OE}$ must be ____(HIGH /LOW) *

(iv) In write operation, $\overline{WE}$ must be _____ (HIGH /LOW) and $\overline{OE}$ must be _____ (HIGH /LOW) *

(v) Given the address input ($A_{14} - A_0$) 101010011100011, the selected row number is _____ and column number is _____ for shift register number_____.

(vi) According to the read cycle timing waveform, the time you must wait after Chip Select CS before valid data are available is _____ns.

(vii) The time taken to write a data into a memory is _____ns.

(viii) The time input data is valid after CS return HIGH for write operation is _____ns.

(b) Read-only memory (ROM) is a class of storage medium used in computers and other electronic devices. Data stored in ROM can only be modified slowly, with difficulty, or not at all. Given in Figure 4 is the internal architecture of a 1024-bit ROM with a 256 x 4 organization based on a 32 x 32 array ROM.

(i) Determine the capacity of the ROM memory

(ii) Determine the number of input address bits and data output bits.

(iii) Draw the logic circuit for ONE of the four 1-of-8 decoders inside the **column decoders** for this ROM. (Hint: Input to the decoders are the address bits and output to the column decoders are Data output)

[10 Marks]
[CO3, PO1,C4]

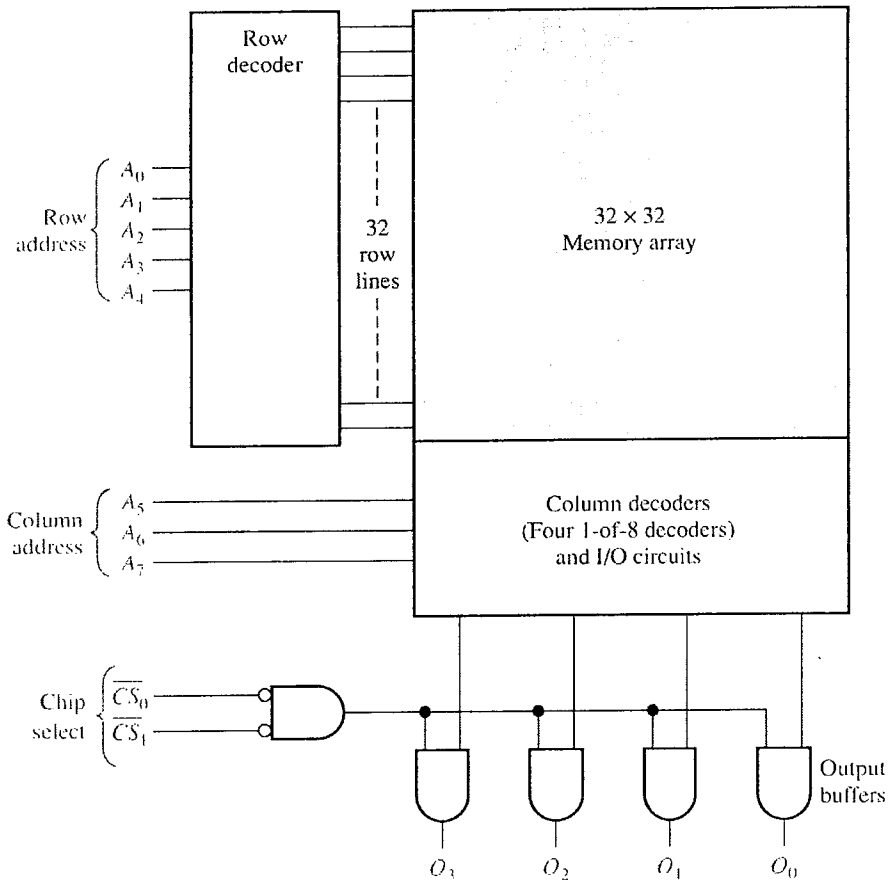

Row
decoder
32 × 32
Memory array
32
row
lines
Row
address
A_0
A_1
A_2
A_3
A_4
Column
address
A_5
A_6
A_7
Column decoders
(Four 1-of-8 decoders)
and I/O circuits
Chip
select
$\overline{CS_0}$
$\overline{CS_1}$
Output
buffers
O_3
O_2
O_1
O_0

Figure 4

PART B: ANSWER ONLY ONE QUESTION

QUESTION 4

(a) Please state/answer each statement with TRUE/FALSE

(i) Clock is the triggering input of a flip-flop.

(ii) SET is the state of a flip-flop or latch when the output is 0.

(iii) A Transparent Latch (gated D latch) must be enabled in order to change state.

(iv) When both J and K inputs are HIGH, an edge-triggered J-K flip-flop changes state on each clock pulse.

(v) Toggle is the action of a flip-flop when it changes state on each clock pulse.

[5 Marks]
[CO2, PO1, C2]

(b) Design a MOD-13 synchronous counter using:

(i) J-K flip-flop

(ii) D flip-flop

[20 Marks]
[CO2, PO1, C4]

QUESTION 5

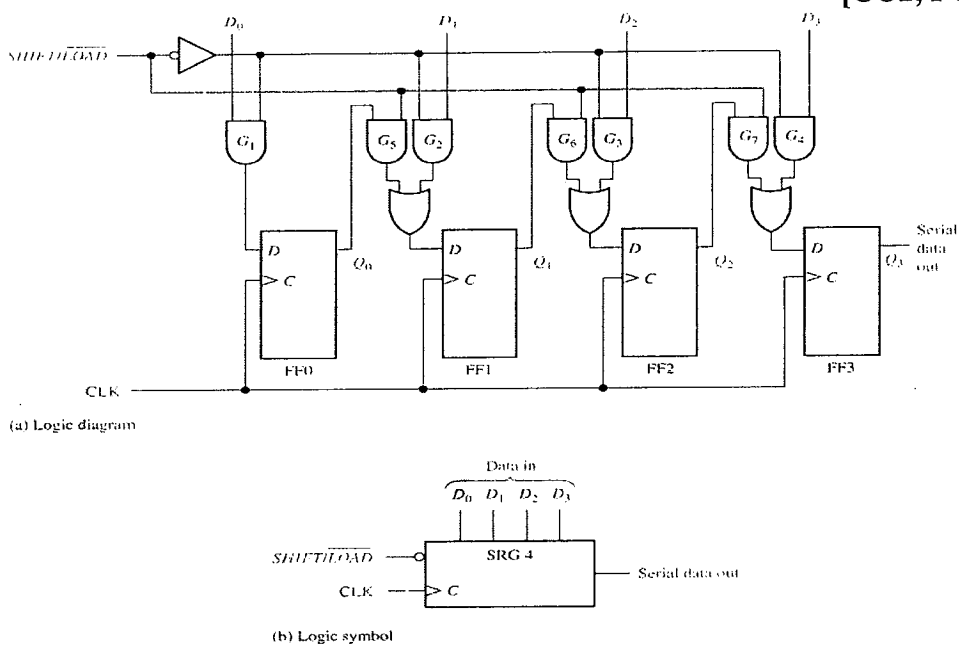
(a) Given in Figure 5 the 4 bits Parallel In/Serial Out (PISO) shift register.

(i) Sketch the waveform diagram to demonstrate the shift register for input 1101.

(ii) Explain the operation of SHIFT/$\overline{LOAD}$ when the input is either HIGH or LOW.

(iii) Which input data bit will appear at the output first? (MSB/LSB) Why?

[8 Marks]
[CO2, PO2, C4]



(a) Logic diagram

(b) Logic symbol

Figure 5

(c) Given in Figure 6 is the logic symbol for 4-bit full adder.

(i) Draw the block diagram of a 4-bit full adder using four full- adder.

(ii) Perform the binary addition of $A = 1001$ and $B = 0011$ using the block diagram that you have drawn.

[11 Marks]
[CO2, PO2, CO3]

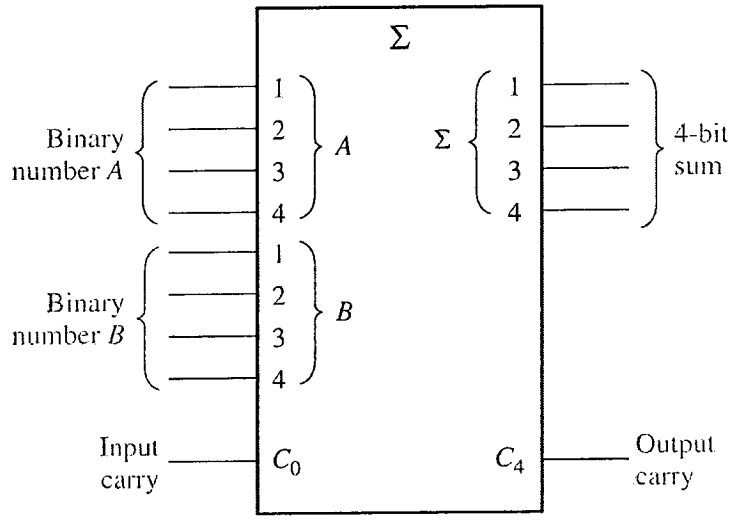


Figure 6

(d) Figure 7 is the BCD-to-7 segment decoder connected to 7 segment display. The input to BCD-to-7 segment decoder is a 4-bits binary A. Sketch the input timing waveform $A = A_3A_2A_1A_0$ if the 7 segment display output sequence is 1,3,9,4,4,4,8,0. Assume A initially zero.

[6 Marks]
[CO2, PO2, CO3]

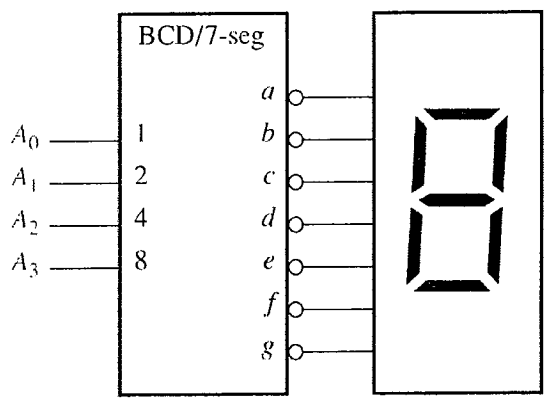


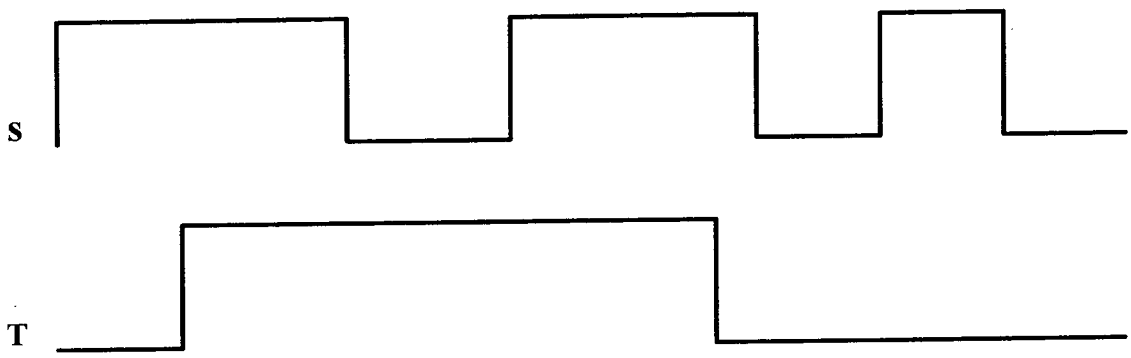
Figure 7

END OF QUESTION PAPER

APPENDIX A

Time waveform for question 2(a)

ID : ____________________ **IC :** ____________________



(i) _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _

(ii) _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _

(iii) _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _

(iv) _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _