Chapter 11

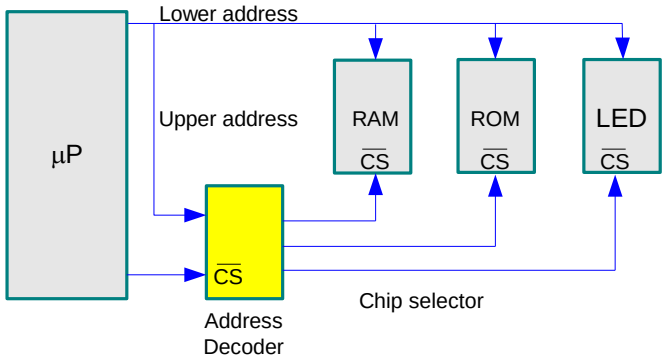
Address Decoder

Expected Outcomes

- Design of address decoder – partial and full
- Interpret and determine address ranges of memory map
- Describe I/O interfacing concept such as I/O driver and memory mapped
- Write a program for simple I/O interfacing

Introduction

- Normally, microprocessor is connected to several devices
- However, only one device can communicate with the processor at one time leaving other devices at high impedance
- To ensure this condition is established, **address decoder** is introduced
- With this decoder, there will not be any devices fighting for control of common wire which may cause damaging to current flow



Address Decoder

- The role of the address decoder is to ensure one device can communicate with the processor at one time.
- This is done by placing all unselected devices into high impedance condition by deactivate enable pin of each device
- There are two type of decoders
  - **Full Address Decoder (FAD)**
    - All address buses of processor must be connected
  - **Partial Address Decoder (PAD)**
    - Only a few selected address buses are connected
      - PAD using combinational circuit
      - PAD using MSI chip

Full Address Decoder

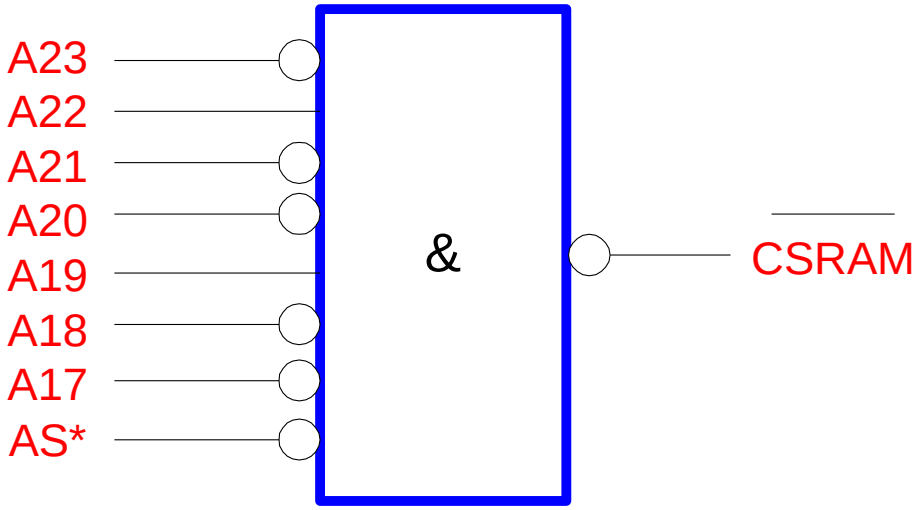
- **Procedure to design the address decoder for memory**
- For each memory device, determine the entire range of address
  - The first address
  - Size of memory
  - The last address
- For each memory device, determine the number of address lines connected to memory
  - Determine the total address lines of the device
  - The lower address lines of processor are connected directly to memory
  - The rest of address lines are connected to the address decoder
- Design decoder circuit

Full Address Decoder

Example

Design a full address decoder for a 128kbyte RAM with the starting address of $480000

Solution



Partial Address Decoder

- **Procedure to design the address decoder for memory**
- For each memory device, determine the entire range of address
  - The first address
  - Size of memory
  - The last address
- For each memory device, determine the number of address lines connected to memory
  - Determine the total address lines of the device
  - The lower address lines of processor are connected directly to memory
  - The rest of address lines can be considered to design the address decoder
  - Normally, higher address lines are used to distinguish devices
  - The less number of lines involved, the simple the decoder circuit

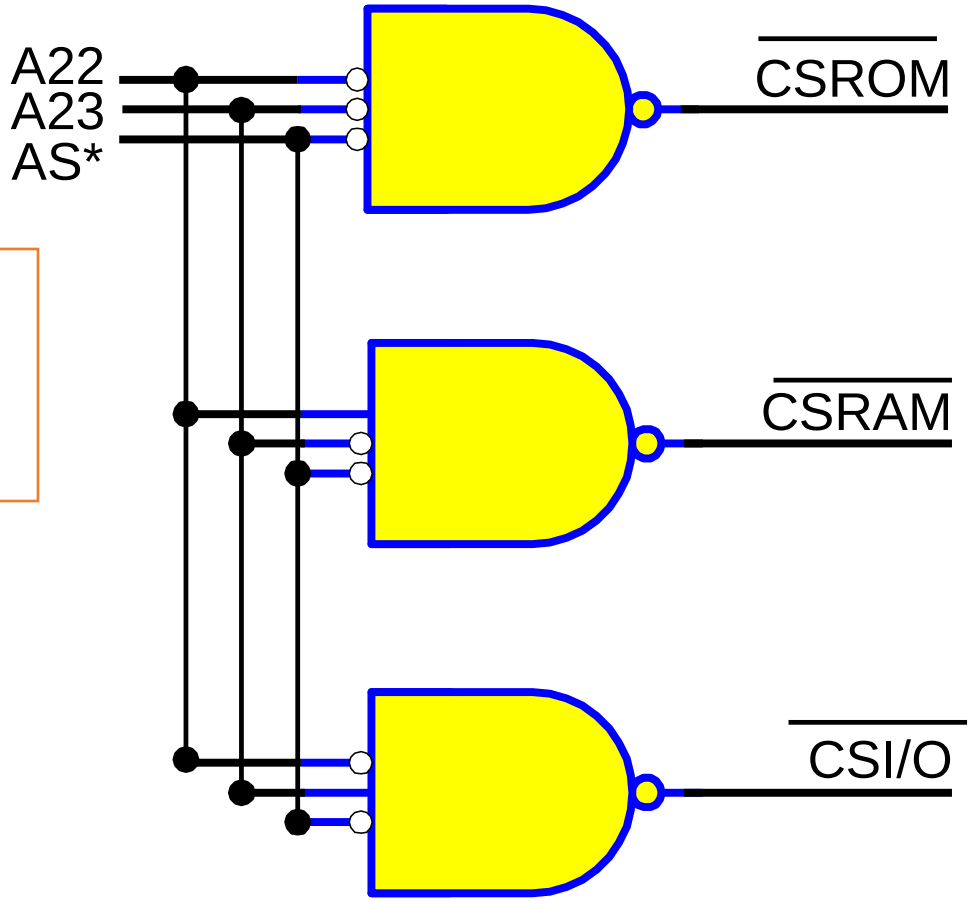
Partial Address Decoder

- **Example**: Design address decoder for following devices
  - RAM (128kbyte) with initial address of $400000
  - ROM (32kbyte) with initial address of $000000
  - I/O with address between $800000 - $80001F

- **Solution**
- RAM is located between $400000 - $49FFFF
- ROM is located between $000000 - $007FFF
- RAM: Address line A0-A16 are connected directly to memory
- ROM: Address line A0-A14 are connected directly to memory
- I/O: Address line A0-A4 are connected directly to I/O device
- Choose the minimum address lines (higher address) to select these devices : A23 and A22

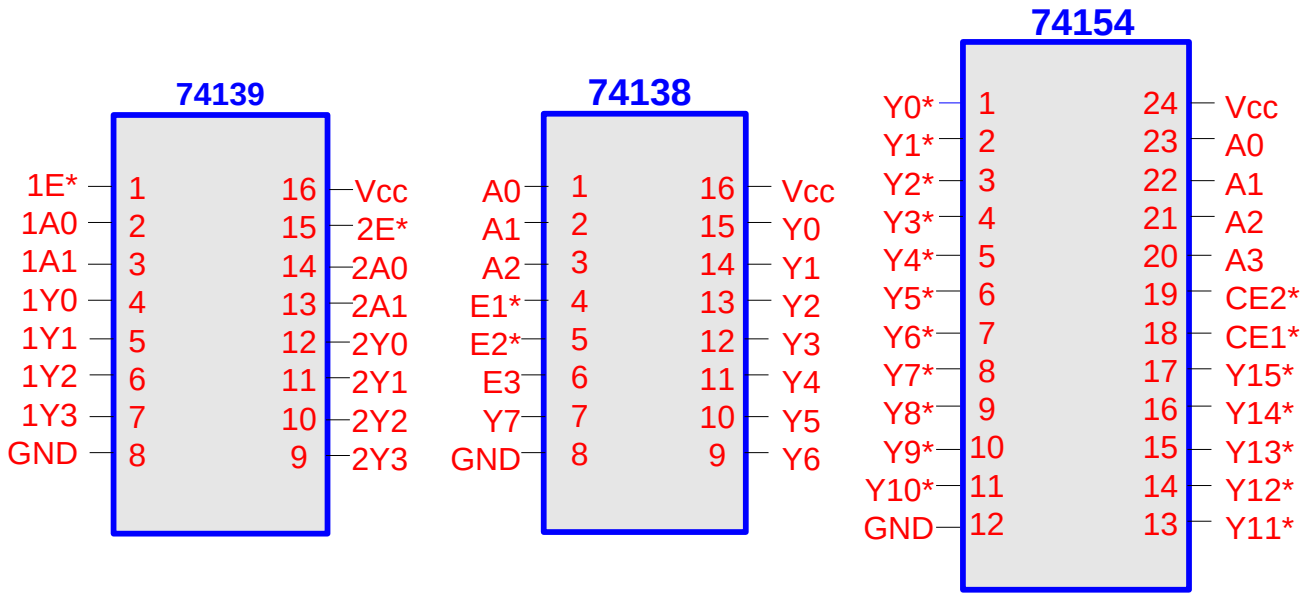
Partial Address Decoder

The address lines are valid when the address strobe (AS) is activated*



MSI

- The most common address decoder using MSI technology are
  - 74139 (2-4 decoder)
  - 74138 (3-8 decoder)
  - 74154 (4-16 decoder)



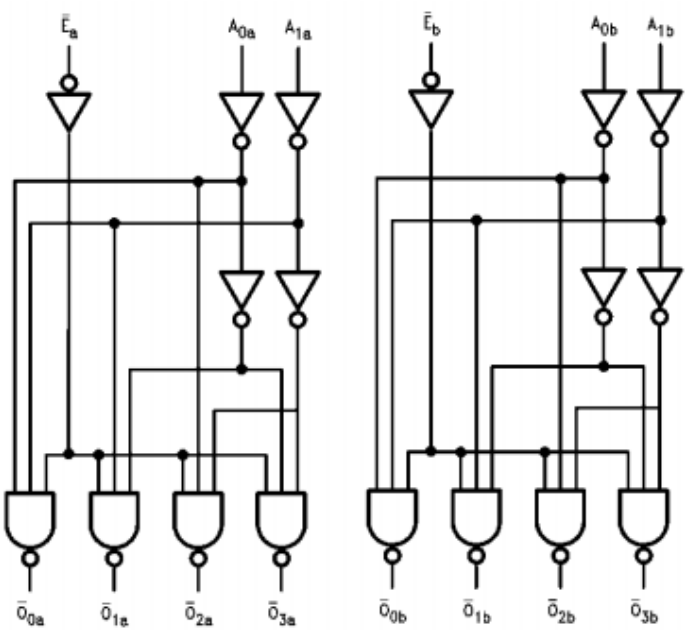
74139

Truth Table

Inputs			Outputs			
$\overline{E}$	A_0	A_1	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram

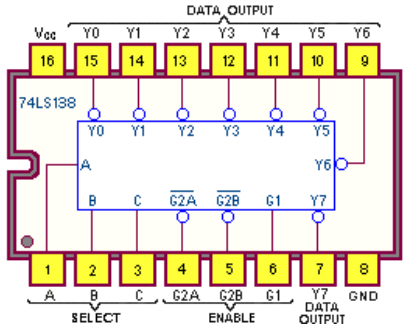


Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

74138

FUNCTION TABLE

ENABLE INPUTS			SELECT INPUTS			OUTPUTS							
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

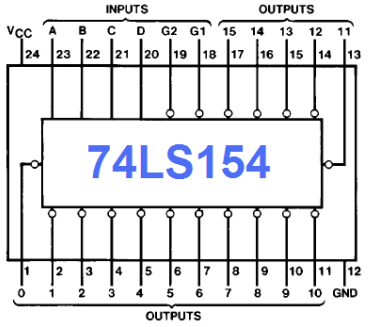


74154

Function Table

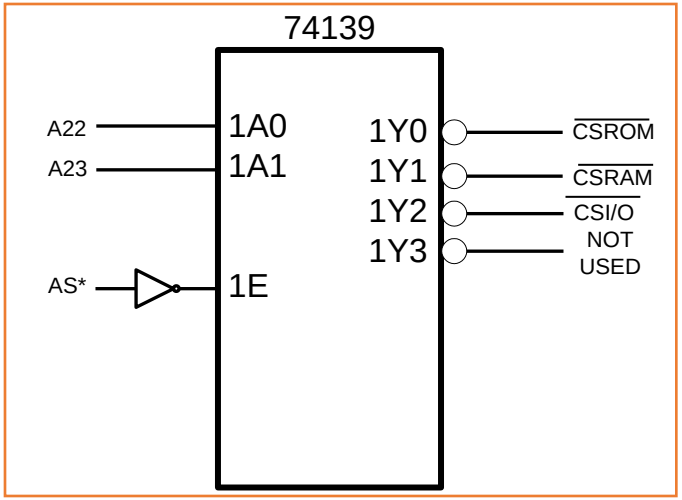
Inputs						Outputs															
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

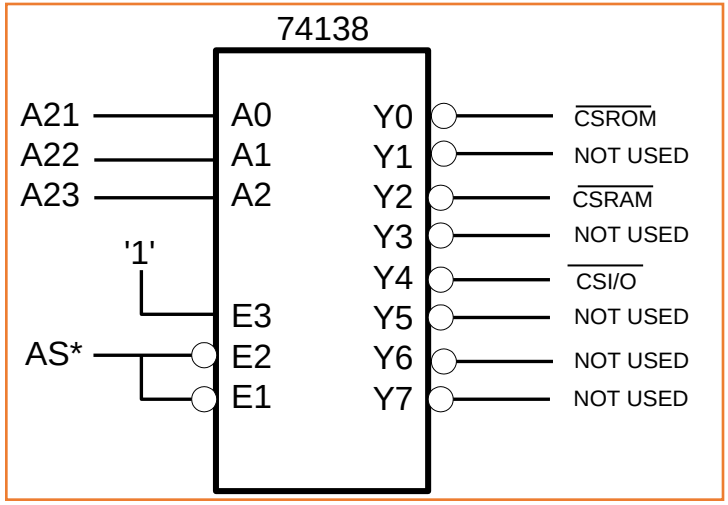
H = High Level, L = Low Level, X = Don't Care



More Examples..

- **Example:** Design address decoder for following devices
  - RAM (128kbyte) with initial address of $400000
  - ROM (32kbyte) with initial address of $000000
  - I/O with address between $800000 - $80001F
- **Solution:**

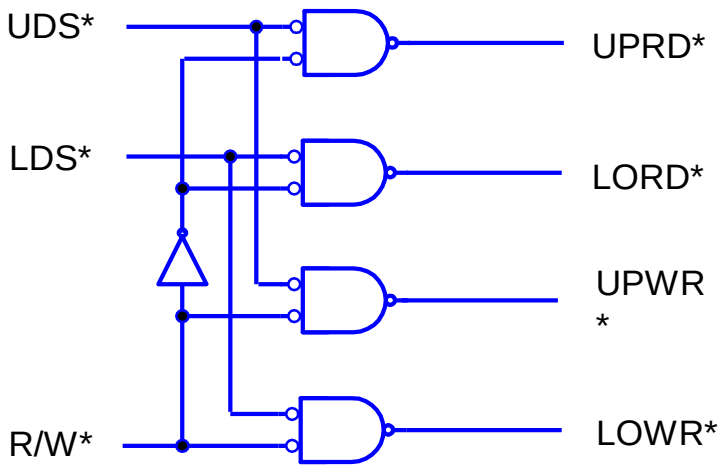




R/W* Control Logic Bus

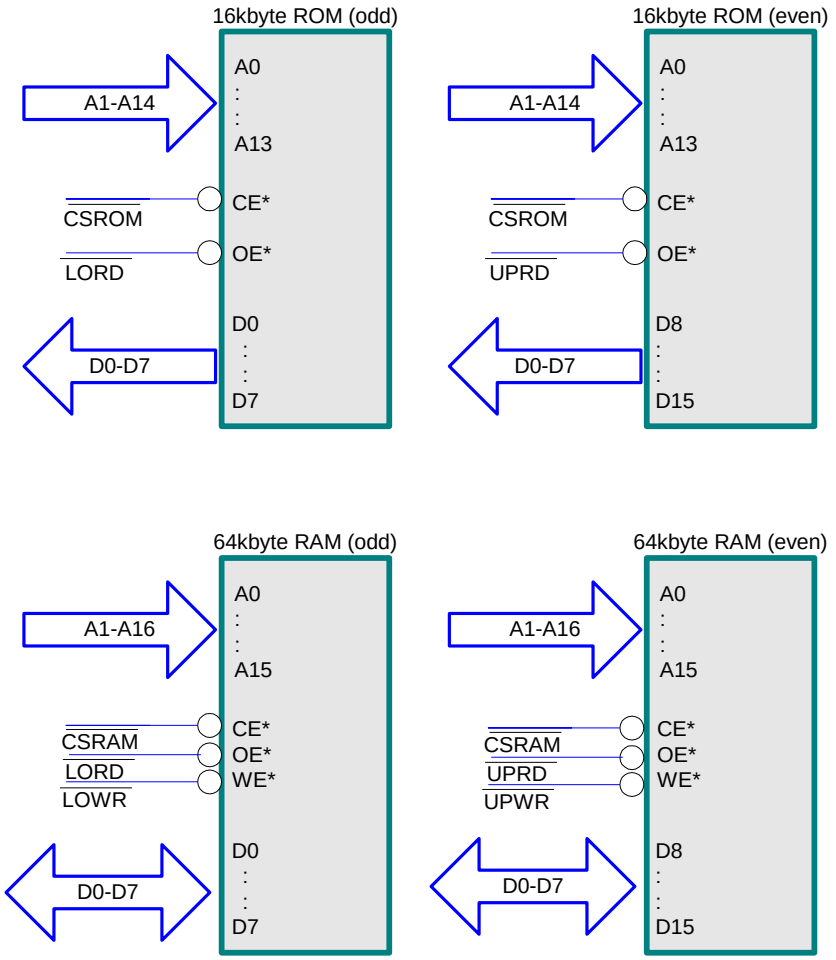
- Control logic for R/W* memory operation

UDS	LDS	R/W	UPRD	LORD	UPWR	LOWR
0	0	0	1	1	0	0
0	0	1	0	0	1	1
0	1	0	1	1	0	1
0	1	1	0	1	1	1
1	0	0	1	1	1	0
1	0	1	1	0	1	1
1	1	0	1	1	1	1
1	1	1	1	1	1	1



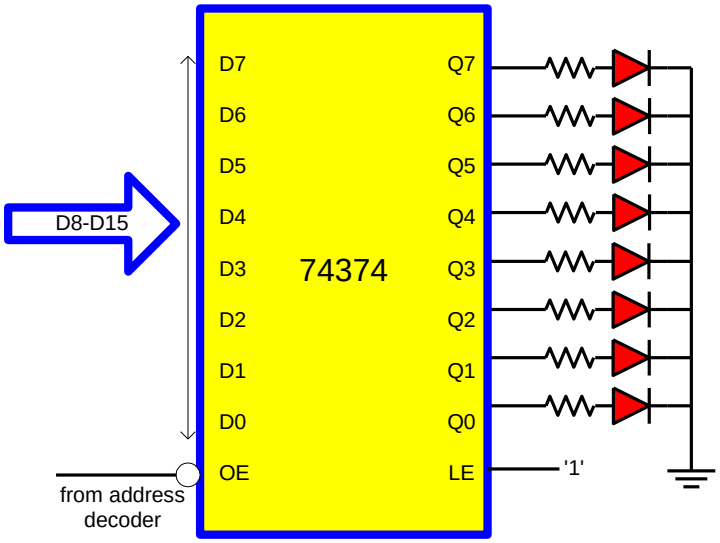
Interface With Memory

- Circuit design from previous example

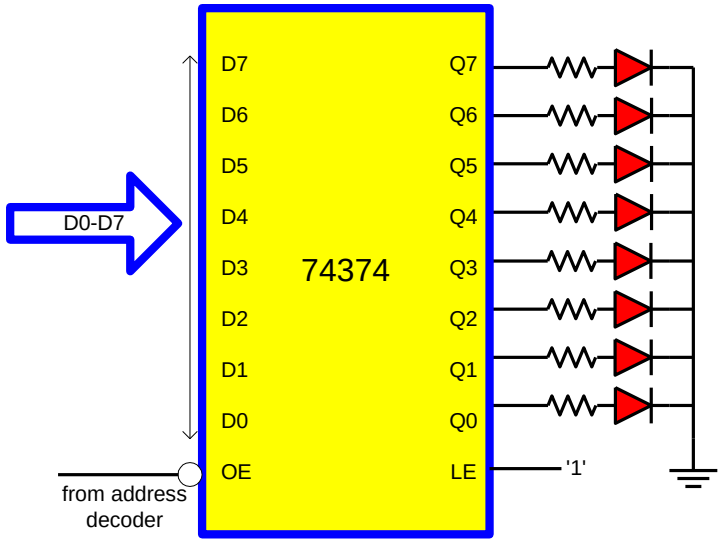


Interface With Latch

- If even address is chosen (simplified circuit)

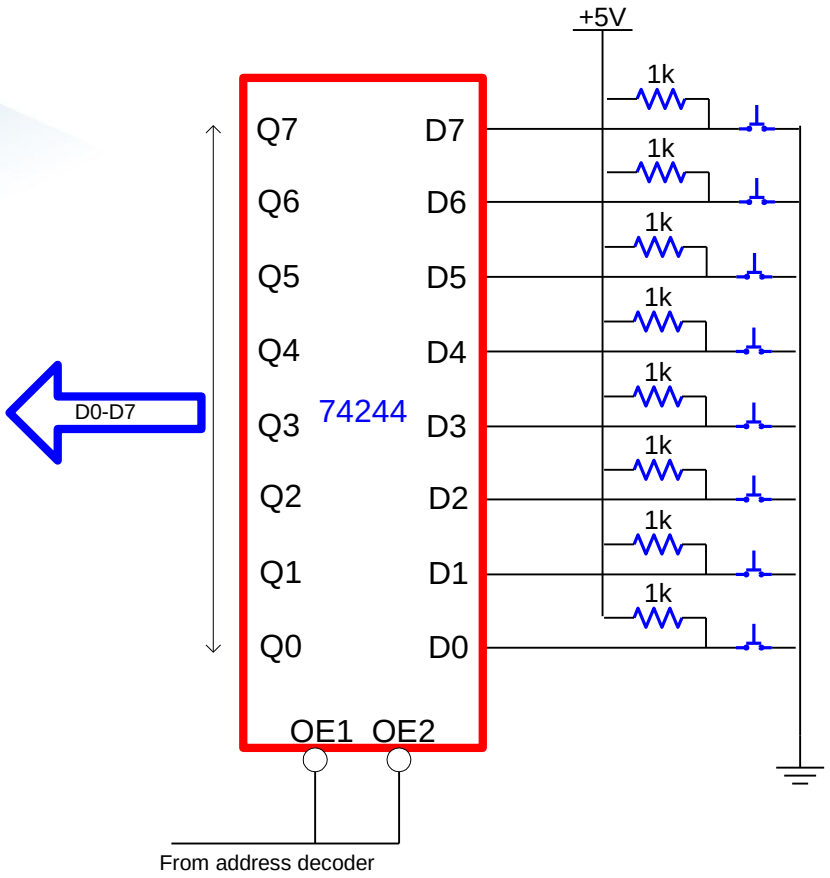


- If odd address is chosen (simplified circuit)

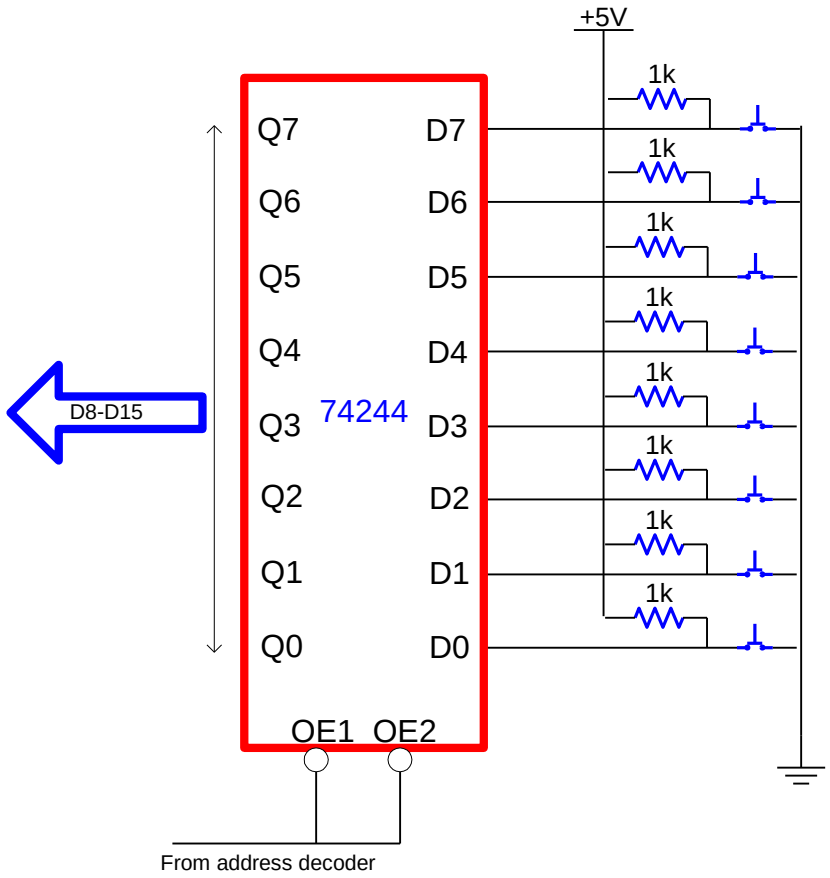


Interface With Buffer

- If odd address is chosen

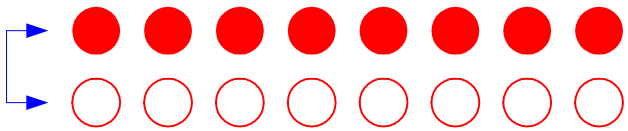


- If even address is chosen



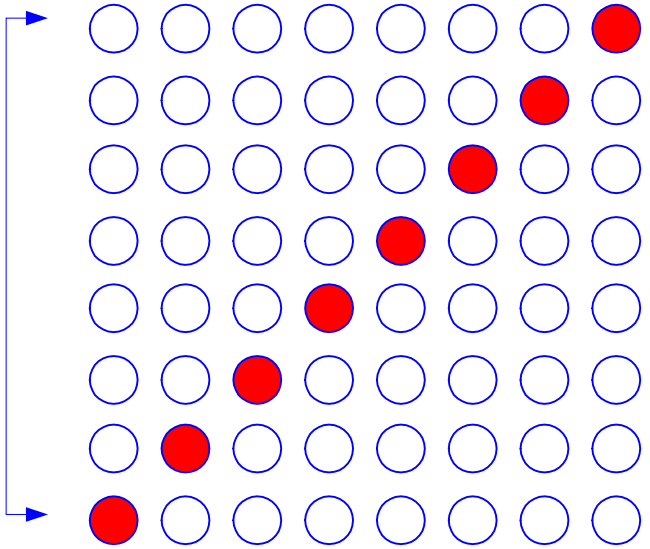
More Examples..

```
LED       EQU       $80000
REPEAT    MOVE.B    #$FF,LED
          BSR       DELAY
          MOVE.B    #0,LED
          BSR       DELAY
          BRA       REPEAT
DELAY     MOVE.L    #$100000,D1
AGAIN     SUBQ.L    #1,D1
          BNE       AGAIN
          RTS
```



More Examples..

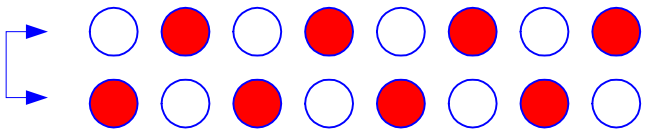
```
LED       EQU    $80000
REPEAT    MOVE.B #1,D0
AGAIN     MOVE.B D0,LED
          BSR    DELAY
          ROL.B  D0
          BCC    AGAIN
          BRA    REPEAT
```



More Examples..

- Write a program to display LED dancing if the RESET switch is pressed. Assume the RESET switch is active low & is located at the LSB of address $90000

```
LED     EQU         $80000
SW1     EQU         $90000
SCAN    MOVE.B      SW1,D0
        ROR.B       #1,D0
        BCS         SCAN
AGAIN   MOVE.B      #$AA,LED
        BSR         DELAY
        MOVE.B      #$55,LED
        BSR         DELAY
        BRA         AGAIN
```



More Examples..

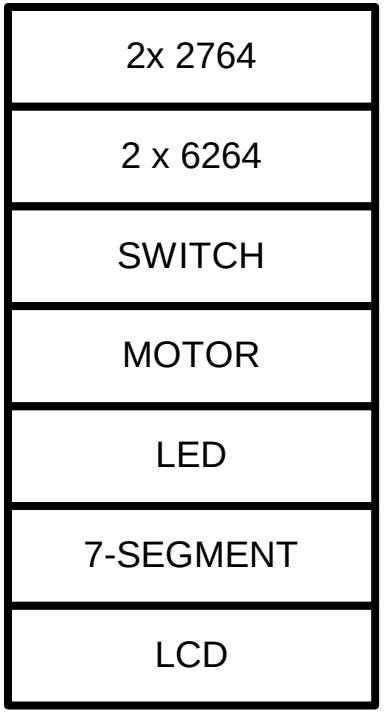
- Write a program to display an upward counter (0,1,2,….8,9,0..) on 7 segment display continuously. Assume the address for 7 segment $400001

```
SEGMENT     EQU         $400001
REPEAT      MOVEA.L     A0,#DATA
            CLR.W       D0
AGAIN       MOVE.B      0(A0,D0),SEGMENT
            ADDQ.W      #1,D0
            CMPI.W      #10,D0
            BNE         AGAIN
            BRA         REPEAT
DATA        DC.B        ……..
```

Self-Test

Exercise

Design a partial decoding circuit that based on memory map given. The design must be based on a (i) 74139 (ii) 74138 and (iii) 74154. Show all the detail of your connections and address ranges for each device.



Self-Test

- **Exercise**

  Write a program to read a byte of data from address of $10000. The data then are inverted and rotate to the right twice and stored back to its original address

- **Exercise**

  If two EPROM 27128 are used and the beginning address of the EPROM is $10000, what is the end address of EPROM?

- **Exercise**

  If address lines of A23-A21 are connected respectively to C, B and A of 74138 with C is MSB, what is the possible address range for the device if Y3* is chosen?

Self-Test

- Exercise

  Write a complete program to meet following requirements,

  - If switch 1 is pressed, the LEDs will blinking continuously
  - If switch 2 is pressed, the LEDs will display free running pattern continuously
  - If switch 3 is pressed, the LEDs will display dancing pattern continuously
  - If switch 4 is pressed, the program is terminated

  Assume that the location of LEDs and switch are $600000 and $800000 respectively