Chapter 10

Memory & Simple I/O Interfacing

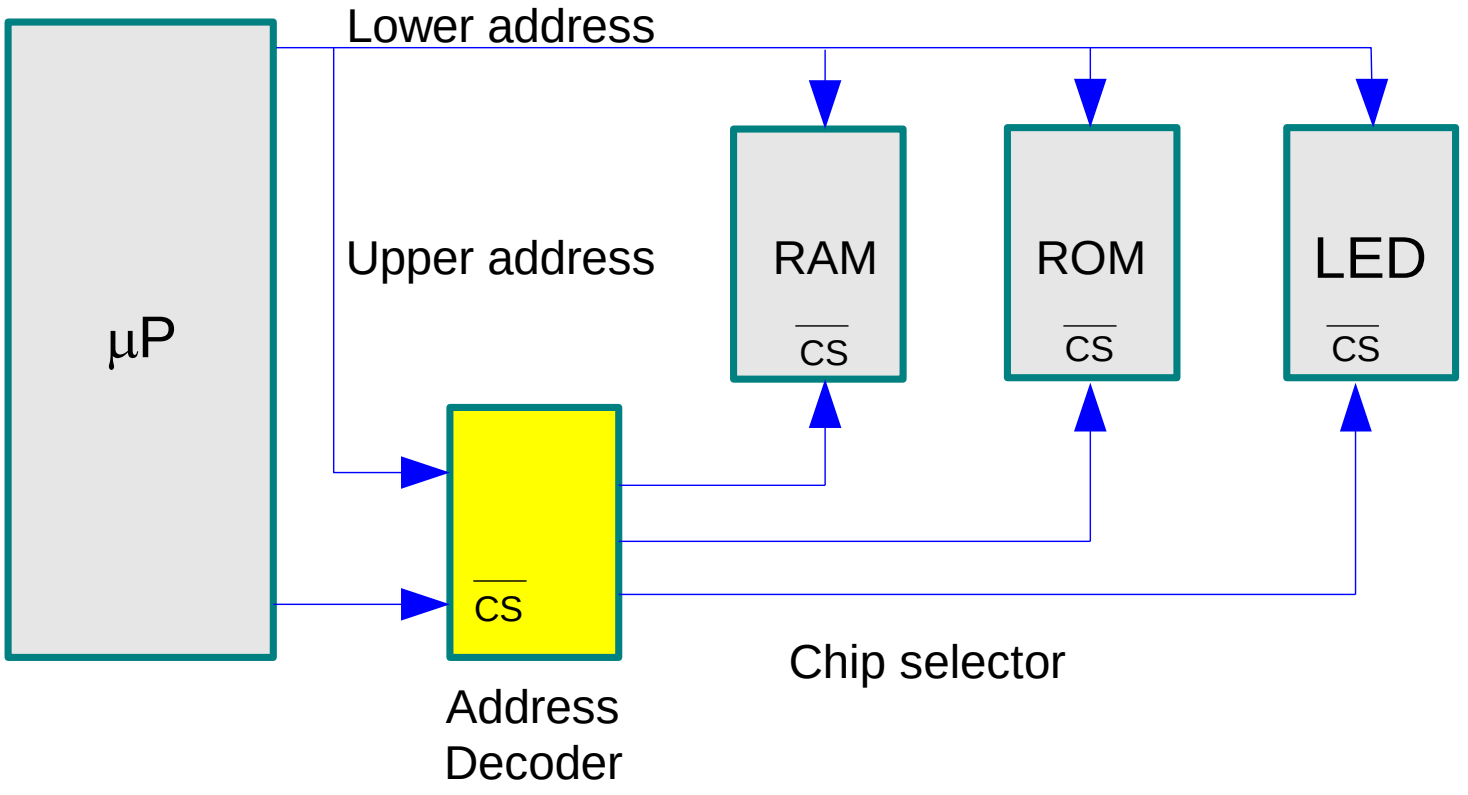
Expected Outcomes

- Explain the importance of tri-state devices in microprocessor system
- Distinguish basic type of semiconductor memory and their applications
- Relate the address and data bus for various memories
- Describe I/O interfacing concept such as I/O driver and memory mapped
- Relate the role of latch and buffer in interfacing with simple I/O devices

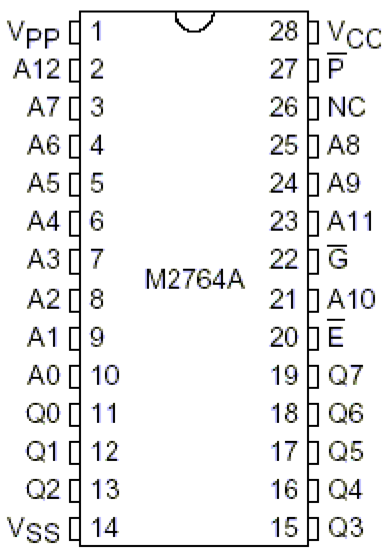
Tri-state Devices

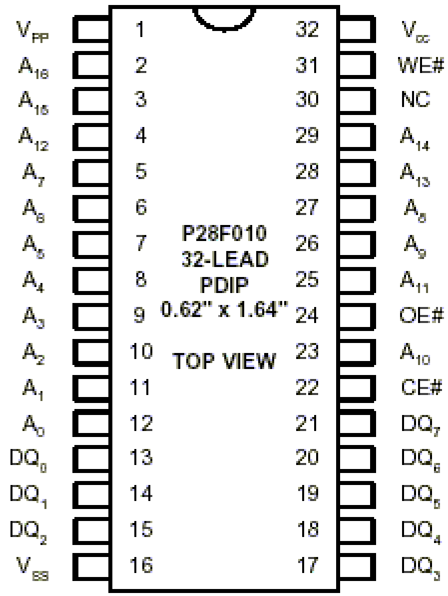
- Any devices connected to a microprocessor should configure in **tristate**
- This is because only **one device** can communicate with the processor at one time leaving other devices at high impedance
- Devices with tristate outputs have an **enable input** such as OE, CS, E, etc
- With this configuration, there will not be any devices fighting for control of common wire which may cause damaging to current flow
- Common devices connected to μP
- Address decoder
  - **Memory** (ROM/RAM)
  - **Input** devices such as keyboard, mouse, switch etc
  - **Output** devices such as printer, monitor, LED, LCD

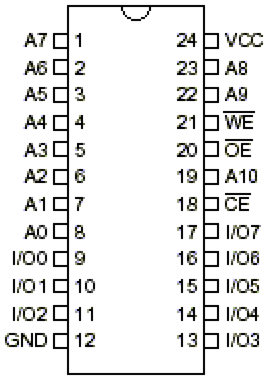
Tri-state Devices

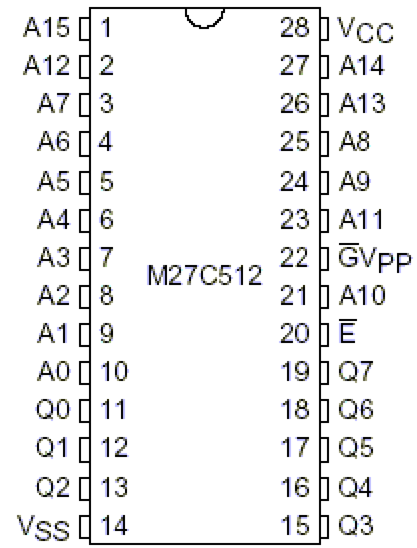


Memory


M2764A
VPP 1 | 28 VCC
A12 2 | 27 P
A7 3 | 26 NC
A6 4 | 25 A8
A5 5 | 24 A9
A4 6 | 23 A11
A3 7 | 22 G
A2 8 | 21 A10
A1 9 | 20 E
A0 10 | 19 Q7
Q0 11 | 18 Q6
Q1 12 | 17 Q5
Q2 13 | 16 Q4
VSS 14 | 15 Q3

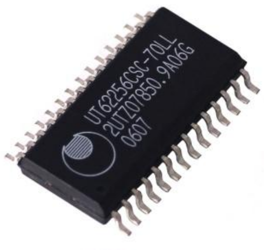

P28F010
32-LEAD
PDIP
0.62" x 1.64"
TOP VIEW
VPP 1 | 32 VCC
A16 2 | 31 WE#
A15 3 | 30 NC
A12 4 | 29 A14
A7 5 | 28 A13
A6 6 | 27 A8
A5 7 | 26 A9
A4 8 | 25 A11
A3 9 | 24 OE#
A2 10 | 23 A10
A1 11 | 22 CE#
A0 12 | 21 DQ7
DQ0 13 | 20 DQ6
DQ1 14 | 19 DQ5
DQ2 15 | 18 DQ4
VSS 16 | 17 DQ3


A7 1 | 24 VCC
A6 2 | 23 A8
A5 3 | 22 A9
A4 4 | 21 WE
A3 5 | 20 OE
A2 6 | 19 A10
A1 7 | 18 CE
A0 8 | 17 I/O7
I/O0 9 | 16 I/O6
I/O1 10 | 15 I/O5
I/O2 11 | 14 I/O4
GND 12 | 13 I/O3


M27C512
A15 1 | 28 VCC
A12 2 | 27 A14
A7 3 | 26 A13
A6 4 | 25 A8
A5 5 | 24 A9
A4 6 | 23 A11
A3 7 | 22 GVPP
A2 8 | 21 A10
A1 9 | 20 E
A0 10 | 19 Q7
Q0 11 | 18 Q6
Q1 12 | 17 Q5
Q2 13 | 16 Q4
VSS 14 | 15 Q3


XICOR


DALLAS


UT62256CSC-70LL

Memory

- Memory system is used to store data and instruction
- Type of memory
  - **ROM (Read Only Memory)**
    - Nonvolatile – data remains even the power is off
    - Normally used to store vectors, self-test routine, monitor program, common subroutine and etc
    - Special device is required to store program in ROM
  - **RAM (Random Access Memory)**
    - Volatile type as data are lost as the power is off
    - Temporary storage and normally used for operation and application system

ROM

- **Programmable Maskable ROM**
  - Very cheap and normally is programmed in factory for mass production
  - One-time written and widely used in game cassette
- **Programmable ROM (PROM)**
  - One-time written and can be programmed by using PROM programmer
- **One-time PROM (OTPROM)**
  - Cheap version of PROM with plastic packed

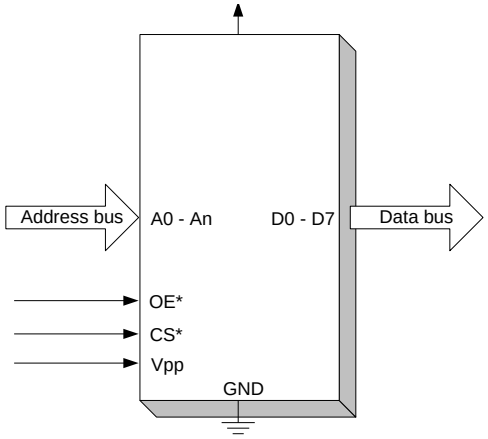
ROM

- **Flash Memory**
  - Like EEPROM, but erasing process involves block-by-block
  - Common in digital camera & MP3

EPROM

Common industrial EPROM

- 2716 2 kbyte (2048 x 8 bits)
- 2732 4 kbyte (4096 x 8 bits)
- 2764 8 kbyte (8192 x 8 bits)
- 27128 16 kbytes (16384 x 8 bits)
- 27256 32 kbytes (32768 x 8 bits)



Common industrial EEPROM

- 2816 2 kbyte (2048 x 8 bits)
- 2864 8 kbyte (8192 x 8 bits)

EPROM

Part No	Capacity	Org	Access	Pins	Vpp
2716	16K	2Kx8	450ns	24	25V
2732	32K	4Kx8	450ns	24	25V
27C32-1	32K	4Kx8	450ns	24	25V CMOS
2764-20	64K	8Kx8	200ns	28	21V
27C64-12	64K	8Kx8	120ns	28	12.5V CMOS
27128-25	128K	16Kx8	250ns	28	21V
27C256-15	256K	32Kx8	150ns	28	12.5V CMOS
27C512-15	512K	6Kx8	150ns	28	12.5V CMOS
27C010-15	1024K	128Kx8	150ns	32	12.5V CMOS
27C020-15	2048K	256Kx8	150ns	32	12.5V CMOS
27C040-15	4096K	512Kx8	150ns	32	12.5V CMOS

EEPROM & Flash Chip

- Some common EEPROM

Part No	Capacity	Org	Speed	Pins	Vpp
2816A-25	16K	2Kx8	250ns	24	5V
2864A	64K	8Kx8	250ns	28	5V
28C64A-25	64K	8Kx8	250ns	28	5V CMOS
28C256-15	256K	32Kx8	150ns	28	5V

- Some common Flash Chips

Part No	Capacity	Org	Speed	Pins	Vpp
28F256-20	256K	32Kx8	200ns	32	12V CMOS
28F010-15	1024K	128Kx8	150ns	32	12V CMOS
28F020-15	2048K	256Kx8	150ns	32	12V CMOS

EPROM Pin Function

- **A0-An (Address Bus)**
  - Address bus directly connected to lower address of microprocessor
- **D0-Dn (Data Bus)**
  - Data bus directly connected to data bus
- **CS* (Chip Select)**
  - To activate EPROM and connected to address decoder
- **OE* (Output Enable)**
  - ROM place data into data bus

EPROM Pin Function

- Vpp
  - Used by EPROM programmer to change bit in the chip
  - Place into high when it is not used

CS*	OE*	Functions
1	0	IC disable with minimum power consumption
1	1	IC disable with minimum power consumption
0	0	Read mode; data are placed on data bus
0	1	Wait state mode; data are placed on the bus when OE* is activated

EPROM Memory Chip

- Examples of Parallel EPROMs

	2716	2732	2764	27128	27256	27512
1			Vpp	Vpp	Vpp	A15
2			A12	A12	A12	A12
3	A7	A7	A7	A7	A7	A7
4	A6	A6	A6	A6	A6	A6
5	A5	A5	A5	A5	A5	A5
6	A4	A4	A4	A4	A4	A4
7	A3	A3	A3	A3	A3	A3
8	A2	A2	A2	A2	A2	A2
9	A1	A1	A1	A1	A1	A1
10	A0	A0	A0	A0	A0	A0
11	D0	D0	D0	D0	D0	D0
12	D1	D1	D1	D1	D1	D1
13	D2	D2	D2	D2	D2	D2
14	GND	GND	GND	GND	GND	GND

	2716	2732	2764	27128	27256	27512
28			Vcc	Vcc	Vcc	Vcc
27			PGM	PGM	A14	A14
26	Vcc	Vcc	N.C	A13	A13	A13
25	A8	A8	A8	A8	A8	A8
24	A9	A9	A9	A9	A9	A9
23	A11	A11	A11	A11	A11	A11
22	OE*	OE*	OE*	OE*	OE*	OE*/Vpp
21	A10	A10	A10	A10	A10	A10
20	CE	CE	CE	CE	CE	CE
19	D7	D7	D7	D7	D7	D7
18	D6	D6	D6	D6	D6	D6
17	D5	D5	D5	D5	D5	D5
16	D4	D4	D4	D4	D4	D4
15	D3	D3	D3	D3	D3	D3

RAM

- Two basic types of RAM
- **Static RAM (SRAM)**
  - Easy to be used and requires an internal flip-flop to store each bit
  - Need 4 – 6 transistor for each FF and suitable for small system
  - 4 times compact than SRAM with the same size
  - Normally used in personal computer
- **Dynamic RAM (DRAM)**
  - Cheaper as dynamic RAM uses a single transistor that acts like a charged capacitor to store each bit
  - Since the charge leaks, a DRAM must use refresh circuit to recharge the capacitor periodically (typically every 2 ms)

RAM & NVRAM

- **Performance difference**
  - DRAM contain more data per chip size
  - SRAM is faster and simpler
- **NV-RAM (Non-volatile RAM)** is introduced to allow the CPU to read and write to it and not lost the content even the power is turned off
- To retain the content, the NVRAM chip internally
  - Uses extremely power efficient – CMOS
  - Uses an internal lithium battery as backup energy
  - Uses intelligent control circuitry to monitor `Vcc` pin and activates internal power if needed
- Thus the NV-RAM is expensive because it must provide the facilities in a single IC

SRAM & DRAM

- Examples of SRAM & DRAM

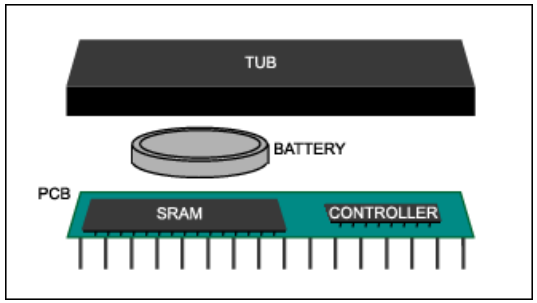
Part No	Capacity	Org	Speed	Pins	Vpp
6116P-1	16K	2Kx8	100ns	24	CMOS
6116LP-3	16K	2Kx8	150ns	24	CMOS
6264P-10	64K	2Kx8	100ns	28	CMOS
62256LP-10	256K	32Kx8	100ns	28	Low Power CMOS
62256LP-12	256K	32Kx8	120ns	28	Low Power CMOS

Part No	Capacity	Org	Speed	Pins
4164-15	64K	64Kx1	150ns	16
41256-15	256K	256Kx1	150ns	16
511000P-8	1M	1Mx1	80ns	18

NVRAM

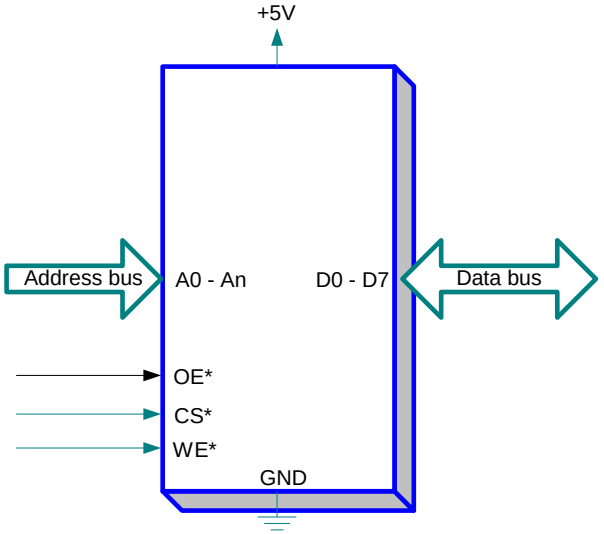
- NV-RAM from Dallas Semiconductor

Part No	Capacity	Org	Speed	Pins
DS1220Y-150	16K	2Kx8	150ns	26
DS1225AB-150	64K	8Kx8	150ns	28
DS1230Y-85	256K	32Kx8	85ns	28



RAM

- Common industrial RAM
  - 6116
    2 kbyte (2048 x 8 bits)
  - 6164/6264
    8 kbyte (8192 x 8 bits)
  - 43256/6625
    32 kbytes (32768 x 8 bits)



RAM

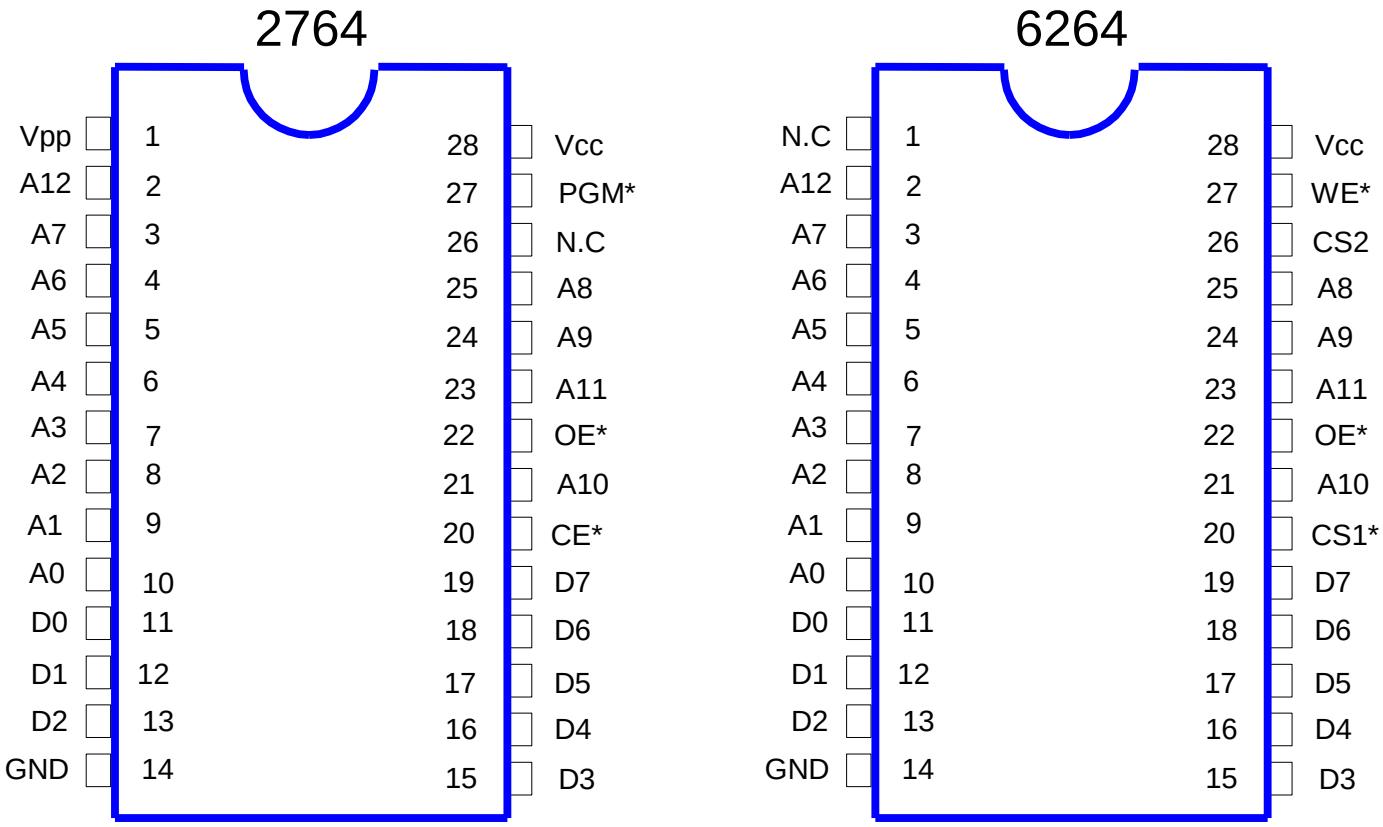
- **A0-An (Address Bus) -** Address bus directly connected to lower address of microprocessor
- **D0-Dn (Data Bus) -** Data bus directly connected to data bus
- **CS* (Chip Select) -** To activate EPROM and connected to address decoder
- **OE* (Output Enable) -** RAM places data into data bus
- **WE* (Write Enable) -** RAM stores data into cell

RAM

- The role of CS*, OE* and WE*

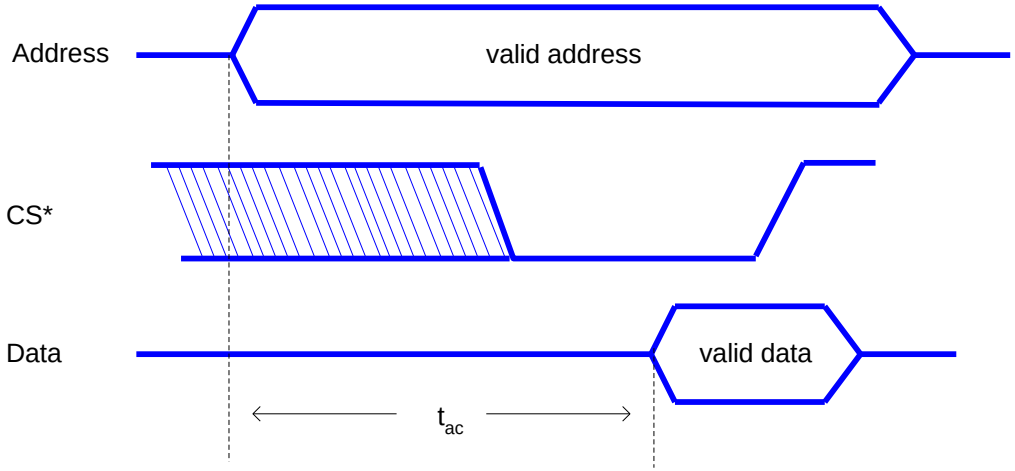
CS*	OE*	WE*	Functions
1	X	X	IC disable with minimum power consumption
0	0	0	Undefined
0	0	1	Read mode; data are placed on data bus
0	1	0	Write mode; data are latched
0	1	1	Wait state mode

2764 vs 6264

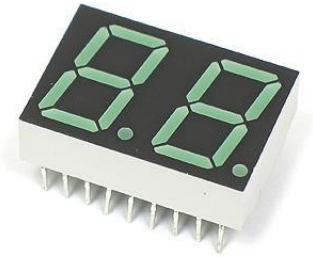

2764
Vpp 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
D0 11
D1 12
D2 13
GND 14
28 Vcc
27 PGM*
26 N.C
25 A8
24 A9
23 A11
22 OE*
21 A10
20 CE*
19 D7
18 D6
17 D5
16 D4
15 D3
6264
N.C 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
D0 11
D1 12
D2 13
GND 14
28 Vcc
27 WE*
26 CS2
25 A8
24 A9
23 A11
22 OE*
21 A10
20 CS1*
19 D7
18 D6
17 D5
16 D4
15 D3

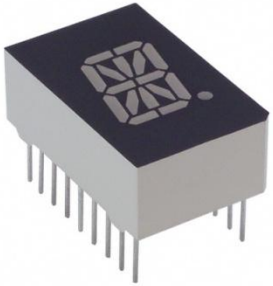
Access Time

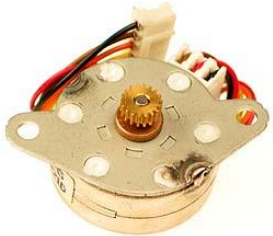
- The performance of memory chips normally are based on access time
- **Access time (t_{ac})** is defined as time taken for the memory to place data onto the data bus as the read signal is received



Simple I/O Devices

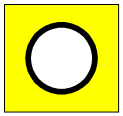


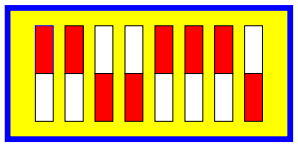


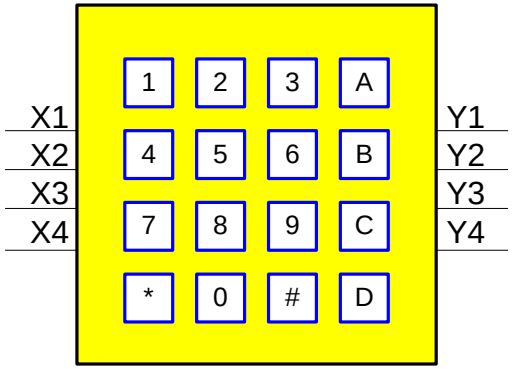


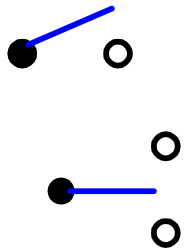
Input Devices

- Most input devices do not possess the tristate configuration
- Normally they are connected to other tristate devices such as buffer to ensure proper interface with μP
- Common input devices
  - Switches (reset, SPST, SPDT etc)
  - Keypad
  - Sensors





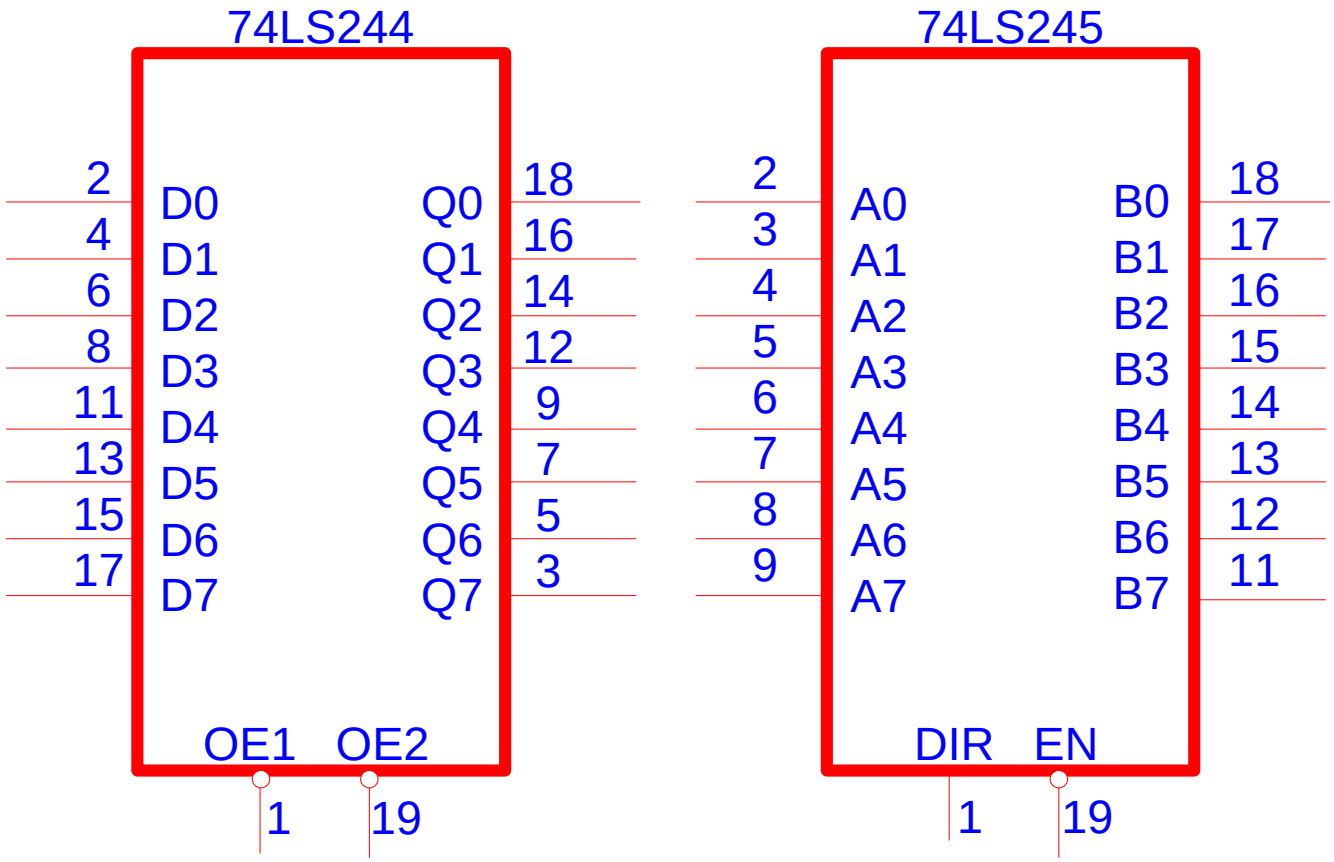




Buffer

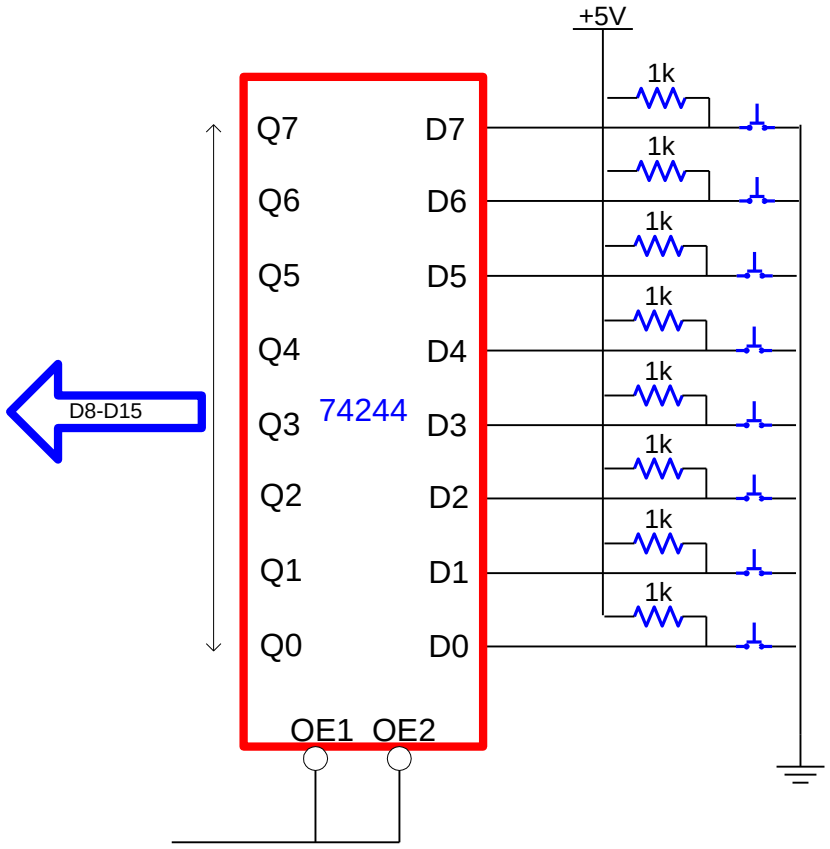
- Buffer is a circuit that allows any logics onto the data bus
- **74LS244 unidirectional tri-state buffer**
  - If OE=0, input is allowed to pass through
  - If OE=1, output is placed in high impedance
- **74LS245 bidirectional buffer**
  - A.k.a transceiver
  - Data direction is determined by DIR
  - If DIR=0, data movement is from A to B
  - If DIR=1, data movement is from B to A

Buffer


74LS244
2
4
6
8
11
13
15
17
D0
D1
D2
D3
D4
D5
D6
D7
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
18
16
14
12
9
7
5
3
OE1
OE2
1
19
74LS245
2
3
4
5
6
7
8
9
A0
A1
A2
A3
A4
A5
A6
A7
B0
B1
B2
B3
B4
B5
B6
B7
18
17
16
15
14
13
12
11
DIR
EN
1
19

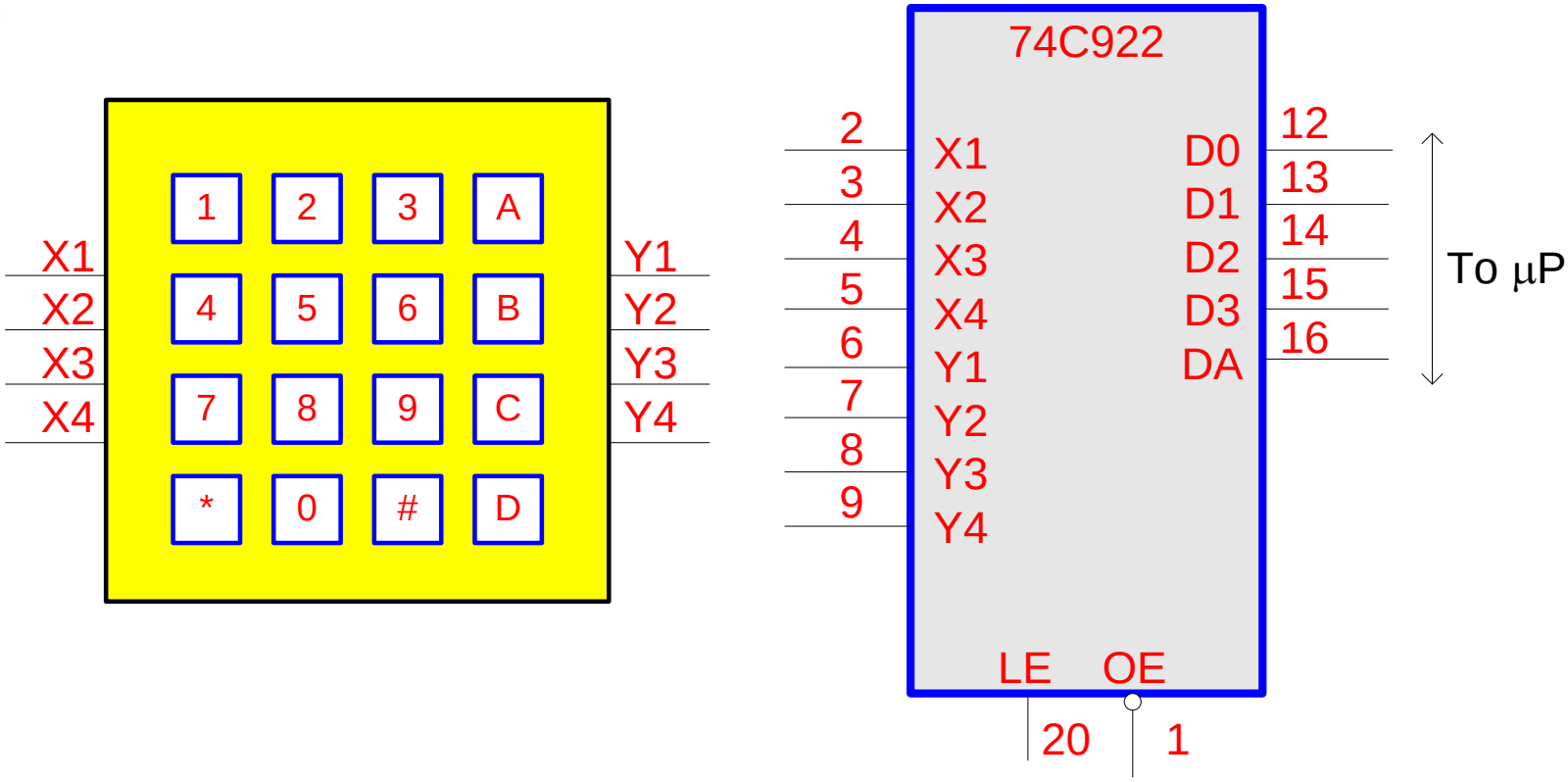
Simple Input Interface

- Simple inputs connection with a buffer
- Enable pins (`OE1*` & `OE2*`) will activate the buffer and normally are connected to address decoder



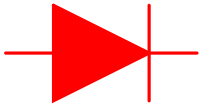
Keypad Encoder

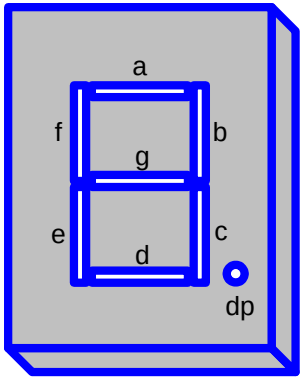
- When a keypad is used in a system, a keypad encoder (74922) is required to facilitate the program

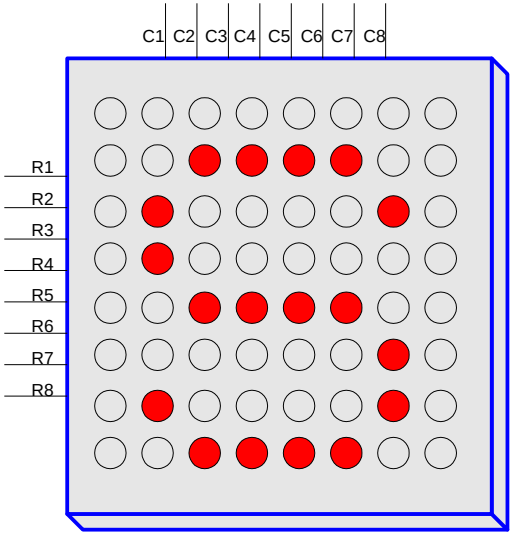


Output Devices

- Like input devices, output devices do not possess the tristate configuration
- They are connected to other tristate devices such as latch for proper interface with processor
- Common output devices
  - Light Emitting Diode (LED)
  - Seven Segment Display
  - Dot Matrix

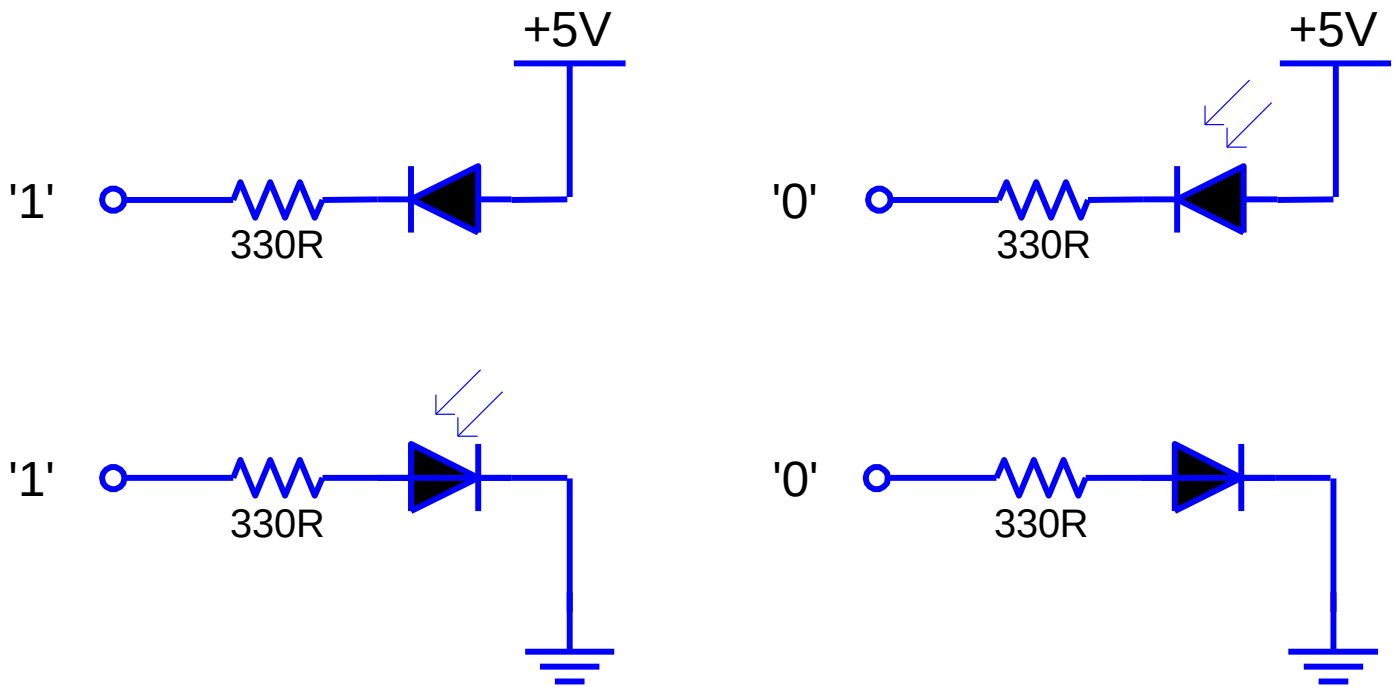






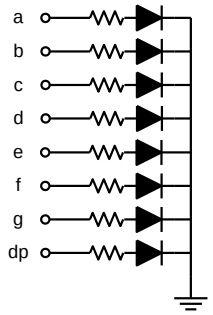
LED

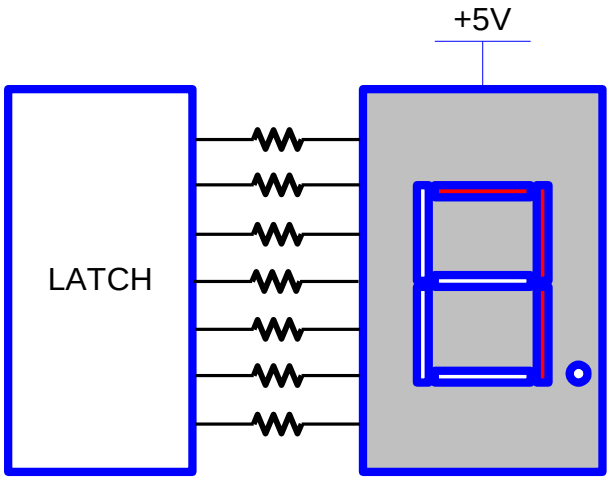
- LED is the most common output device used in microprocessor-based system due its simplicity & cost



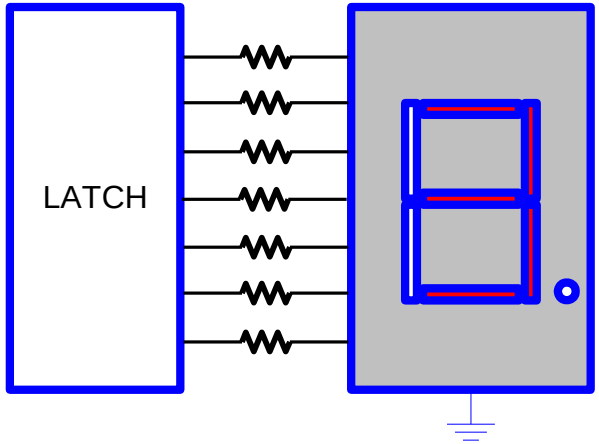
7-Segment Display

- There two type configurations
  - Common Anode
  - Common Cathode





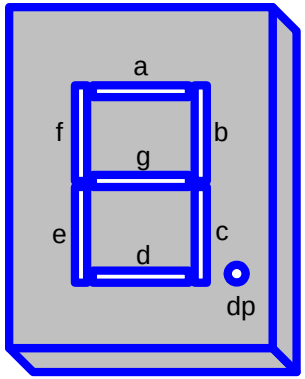
Common Anode

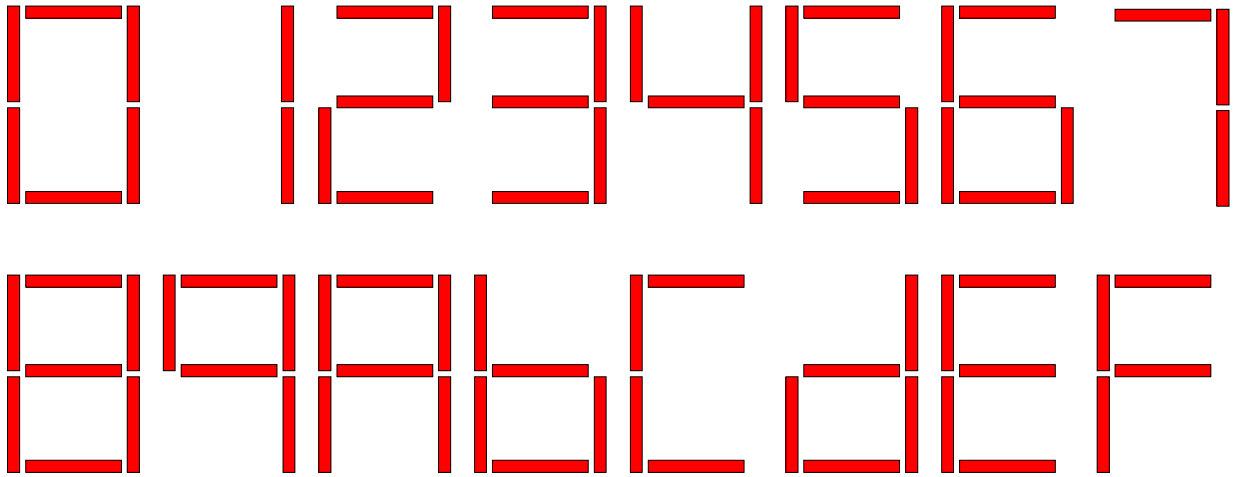


Common Cathode

7-Segment Display

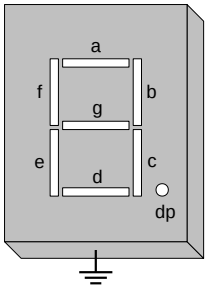
- Common Cathode
- Common Anode





7-Segment Display

Common Cathode



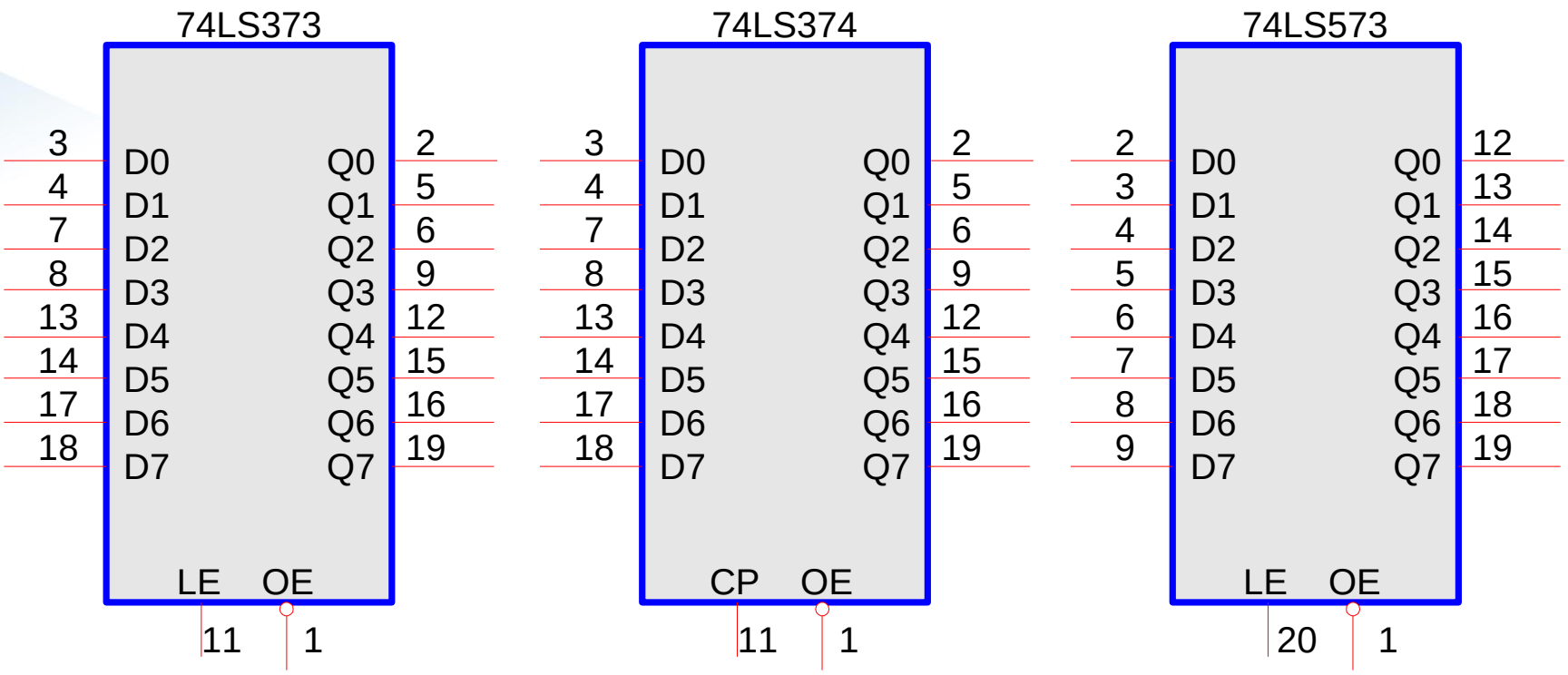
	a	b	c	d	e	f	g
0	1	1	1	1	1	1	0
1	0	1	1	0	0	0	0
2	1	1	0	1	1	0	1
3	1	1	1	1	0	0	1
4	0	1	1	1	0	0	1
5	1	0	1	1	0	1	1
6	1	0	1	1	1	1	1
7	1	1	1	0	0	0	0

	a	b	c	d	e	f	g
8	1	1	1	1	1	1	1
9	1	1	1	0	0	1	1
A	1	1	1	0	1	1	1
B	0	0	1	1	1	1	1
C	1	0	0	1	1	1	0
D	0	1	1	1	1	0	1
E	1	0	0	1	1	1	1
F	1	0	0	0	1	1	1

Latch

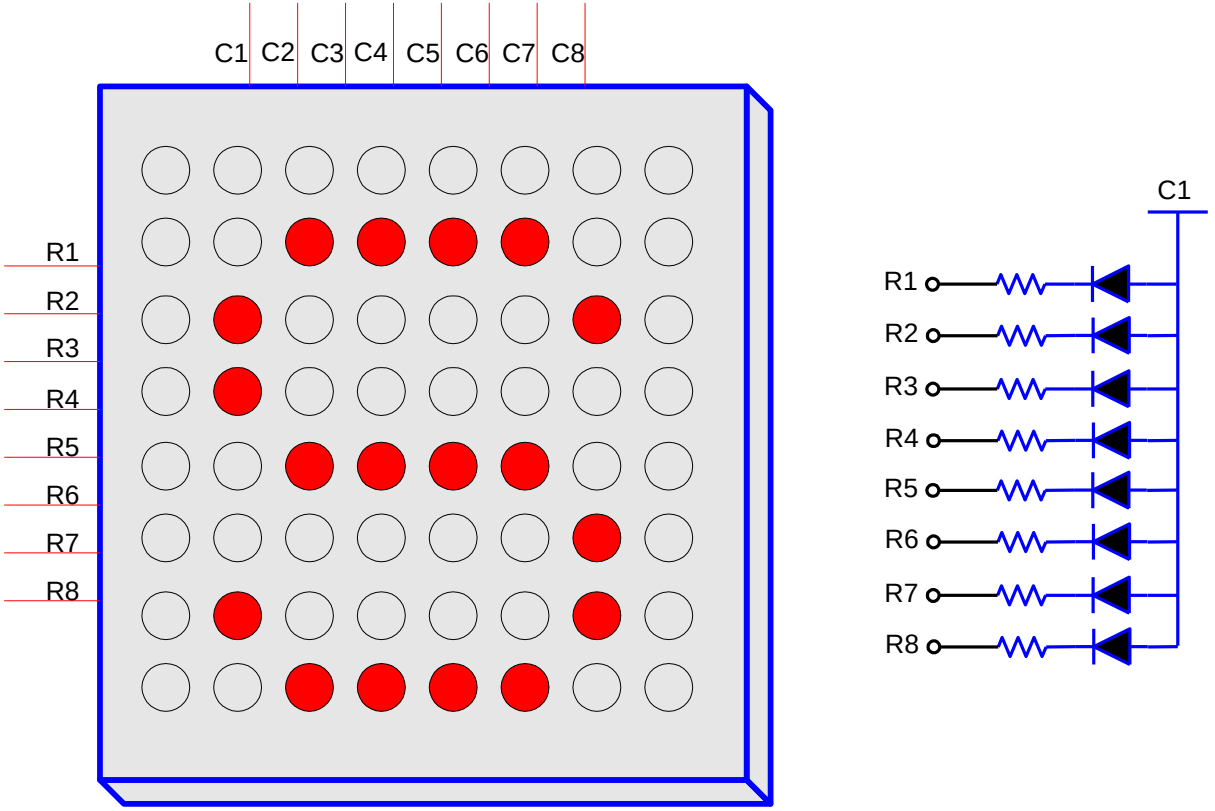
- Latch is a circuit that capture value at the input
- **74LS373 transparent latch**
  - During `LE=1`, Q=D
  - During `LE=0`, Q hold D during negative edge
  - Another version is 74LS573 where the difference is in pin configuration
- **74LS374 edge triggering**
  - During positive transition at `CP`, data is transferred from D to Q
  - Another version is 74LS574 where the difference is in pin configuration

Latch


74LS373
3 D0
4 D1
7 D2
8 D3
13 D4
14 D5
17 D6
18 D7
Q0 2
Q1 5
Q2 6
Q3 9
Q4 12
Q5 15
Q6 16
Q7 19
LE 11
OE 1
74LS374
3 D0
4 D1
7 D2
8 D3
13 D4
14 D5
17 D6
18 D7
Q0 2
Q1 5
Q2 6
Q3 9
Q4 12
Q5 15
Q6 16
Q7 19
CP 11
OE 1
74LS573
2 D0
3 D1
4 D2
5 D3
6 D4
7 D5
8 D6
9 D7
Q0 12
Q1 13
Q2 14
Q3 15
Q4 16
Q5 17
Q6 18
Q7 19
LE 20
OE 1

Dot Matrix

- A multi-purpose output display, dot matrix is another common output device



Self-Test

- Determine the number of address pins and memory capacity of the following EPROM

Part No	Capacity (bytes)	Address Pins
TMS27C64		
HD2716		
NM27C128		
62256LP-10		
27C010-15		
27C040-15		
27512-25		

Self-Test

Exercise

For ROM chip 27128, find the number of data and address pins. In your opinion what is the minimum pin configuration of the chip

Exercise

Discuss the number of pins for addresses in (i) 2 kbytes RAM (ii) 512 bytes of RAM

Exercise

Explain the difference between EEPROM and flash memory

Exercise

Which memory is used as cache memory in the PC?

Self-Test

- **Exercise**

  Explain the role of `OE*`, `CS*`, `WE*` pins in RAM

- **Exercise**

  Why do we need to use latch instead of connecting the output device (such as 7-segment display) directly to the CPU?

- **Exercise**

  What is access time for a memory? Briefly describe the important of fast access time in a microprocessor system by giving an example