



Chapter 2

Introduction to 68000

Expected Outcomes

Point out the feature of 68000 and its architecture
 Recognize the register sets in 68000 programming model
 Interpret the memory map and its addressing ranges



Introduction

- MC68000 is one of the most popular microprocessor as its instruction set is comprehensive and its design is simple for 16 bit system.
- It is capable of supporting multitasking and applicable for high level language
- It uses Von Neumann architecture to produce a simple and flat memory map
- Originally, it is designed for use in household products
- But later, it is used for the design of computers like the Apple Macintosh, Commodore Amiga and Atari ST
- The 68000 eventually obtains it greatest success as a controller such as in HP and Adobe printer
- Its derivatives such as Coldfire have been manufactured for the use of automotive engine controller.





Evolution

- The first microprocessor for Motorola is MC6800 introduced in 1974. This included 6802, 6808,6809 and 6805
- MACSS introduced MC68000 in 1979 with 16 bit data bus and can be operated with 32 bit (16/32 bits)
- Other upgraded family such as 68020, 8030, 68040 and 68060 upward compatible
- Also known as 680x0 or 68k
- Motorola ceased production of original NMOS 68000 in 2000 although its derivative such as 68HC00 is still continued in production
- As of 2001, Hitachi and other manufactures continue to manufacture the 68000 under license





68000 Manufacturer

| Manufacturer | Description | | | |
|--------------------------|---------------------------------------|--|--|--|
| Apple 68000-8 | 8 MHz, 64-pin side-brazed ceramic DIP | | | |
| Hitachi HD68000-8 | 8 MHz, 64-pin side-brazed ceramic DIP | | | |
| Mostek MK68000-8B | 8 MHz, 64-pin plastic DIP | | | |
| Motorola XC68000L | 64-pin side-brazed ceramic DIP | | | |
| Rockwell R68000C8 | 8 MHz, 64-pin side-brazed ceramic DIP | | | |
| SGS-Thompson TS68000CP10 | 10 MHz, 64-pin plastic DIP | | | |
| Signetics SCN68000C4164 | 4 MHz, 64-pin side-brazed ceramic DIP | | | |
| Thompson TS68000CFN16 | 16 MHz, 68 Lead plastic LCC | | | |
| Toshiba TMP68HC000P-10 | 10MHz, 64-pin plastic DIP | | | |
| Motorola MC68HC000LC8 | 8 MHz, 64-pin side-brazed ceramic DIP | | | |
| Hitachi HD68000Y10 | 10 MHz, 68-pin ceramic PGA | | | |





68000 General Specification

Specifications
32-bit Data and Address Registers
16-bit Data Bus
24-bit Address Bus
14 Addressing Modes
Memory-Mapped Input/Output
Program Counter
56 General Instruction Sets
5 Main Data Types
7 Interrupt levels
Synchronous and asynchronous data transfer

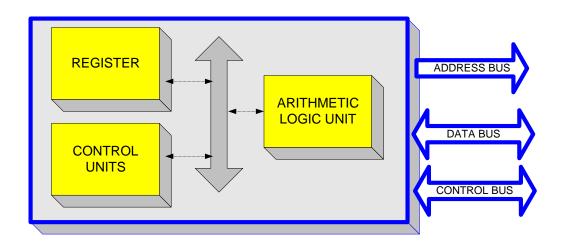






68000 Architecture

68000 consists of three main modules
 Registers
 Arithmetic Logic Unit (ALU)
 Control Unit







68000 Registers

8 Data Registers (D0 – D7) Data storage with 8, 16, and 32 bits operation 8 Address Registers (A0 – A7) Address storage with 16 or 32 bits

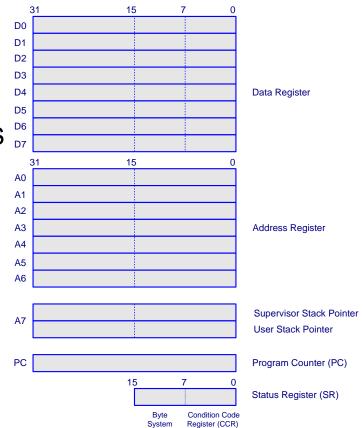
Address storage with 16 or 32 bits operation

A7 also known as Stack Pointer
 Program Counter (PC)

Represent the next address of instruction

Status Register (SR)

 Consists of byte system and Condition code register (CCR)
 Information of result due to execution of instruction
 Instruction Register (IR)







Status Register

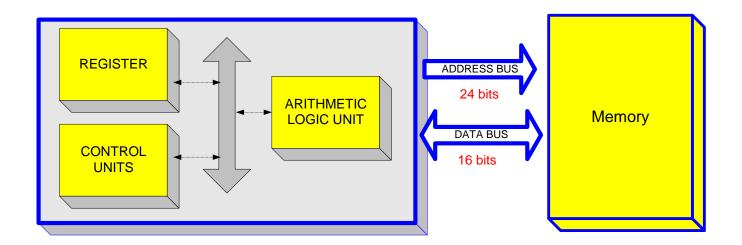
| Bit | | Desc | riptic | on | | | | | | | | | | |
|-------|------|---|--------|----|----|----|---|---|---|---|---|---|---|---|
| Т | | Tracing for run-time debugging | | | | | | | | | | | | |
| S | | Supervisor or User mode | | | | | | | | | | | | |
| I | | System responds to interrupts with a level higher than I | | | | | | | | | | | | |
| X | | Retains information from carry bit for multi precision arithmetic | | | | | | | | | | | | |
| N | | Set if the result is MSB is set | | | | | | | | | | | | |
| Z | | Set if the result is zero | | | | | | | | | | | | |
| V | | Set if a signed overflow occur | | | | | | | | | | | | |
| C | | Set if a carry or borrow is generated | | | | | | | | | | | | |
| 15 14 | 4 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Т | S | | | 12 | 11 | 10 | | | | Χ | Ν | Ζ | V | С |





68000 & Memory

Every byte in memory is assigned with an address
 Memory size depends on the size of address bus
 Address range that can be accessed by N bus is 0 to 2^{N-1}
 68000 has 24 bits, thus it has 16 777 216 byte location





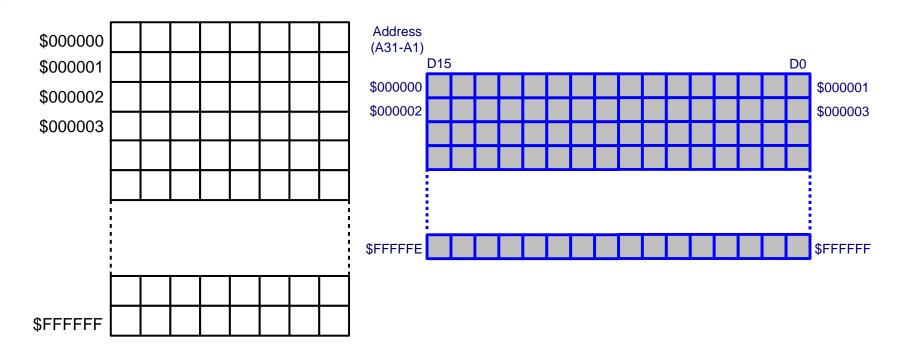


Memory Map

24-bit addresses—16MB memory available

Reorganize due to 16-bit data bus

Content of a location







Byte Addressing

- 68000 can read/write data in byte form as the data bus width is 16 bit
- Thus byte can be placed anywhere in memory

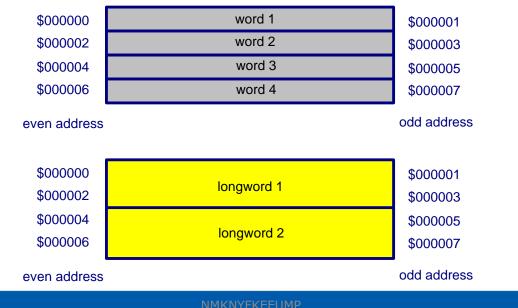
| \$000000 | byte 0 | byte 1 | \$000001 |
|----------|--------|--------|----------|
| \$000002 | byte 2 | byte 3 | \$000003 |
| \$000004 | byte 4 | byte 5 | \$000005 |
| \$000006 | byte 6 | byte 7 | \$000007 |





Word & Long-word Addressing

- 68000 can read/write data in word form as the data bus width is 16 bit
- Thus word operation must start at even address
- High byte is placed in even address and the lower byte is in odd address
- Similarly, long-word operation must begin at even address







68000 Family

MC68000 – 16/32 Bit Microprocessor MC68EC000 – 16/32 Bit Embedded Controller MC68HC000 – Low Power 16/32 Bit Microprocessor MC68008 – 16-Bit Microprocessor with 8-Bit Data Bus MC68010 – 16/32 Bit Virtual memory Microprocessor MC68020 – 32 Bit Virtual memory Microprocessor MC68EC020 – 32 Bit Embedded Controller MC68030 – 2nd Generation 32 Bit Microprocessor MC68EC030 – 32 Bit Embedded Controller MC68040 – 3rd Generation 32 Bit Microprocessor





68000 Family

- MC68LC040 3rd Generation 32 Bit Microprocessor
- MC68EC040 32 Bit Embedded Controller
- MC68060 MC68040 with exceptional performance
- MC68LC060 MC68060 with no FPU (Floating Point Unit)
- MC68330 Integrated CPU32 Processor
- MC68340 Integrated Processor with DMA
- MC68881 Floating Point Processor
- MC68882 Enhanced Floating Point Processor
- MC68302 MC68EC00 with internal DRAM, serial/parallel and timer





Self-Test

Exercise

Describe the READ operation in computer system

Exercise

What is the size of data bus and address bus of MC68000 ?

Exercise

If a processor has 8-bit data bus and 16-bit of address bus, what is possible size of the memory ?

Exercise

Why the address bus of A0 is not part of MC68000 pin configuration?

