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BFF1303: ELECTRICAL / ELECTRONICS ENGINEERING

Analog Electronics: BJT Biasing Circuits

Ismail Mohd Khairuddin , Zulkifil Md Yusof
Faculty of Manufacturing Engineering
Universiti Malaysia Pahang

Bipolar Junction Transistor-DC Biasing

BFF1303 ELECTRICAL/ELECTRONICS ENGINEERING

Faculty of Manufacturing

Universiti Malaysia Pahang
Kampus Pekan, Pahang Darul Makmur
Tel: +609-424 5800
Fax: +609-4245888

http://fkp.ump.edu.my/

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- Design Operations
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Outcomes

Understand the physical operation of bipolar transistor

→ Select the operating point of a bipolar transistor circuit

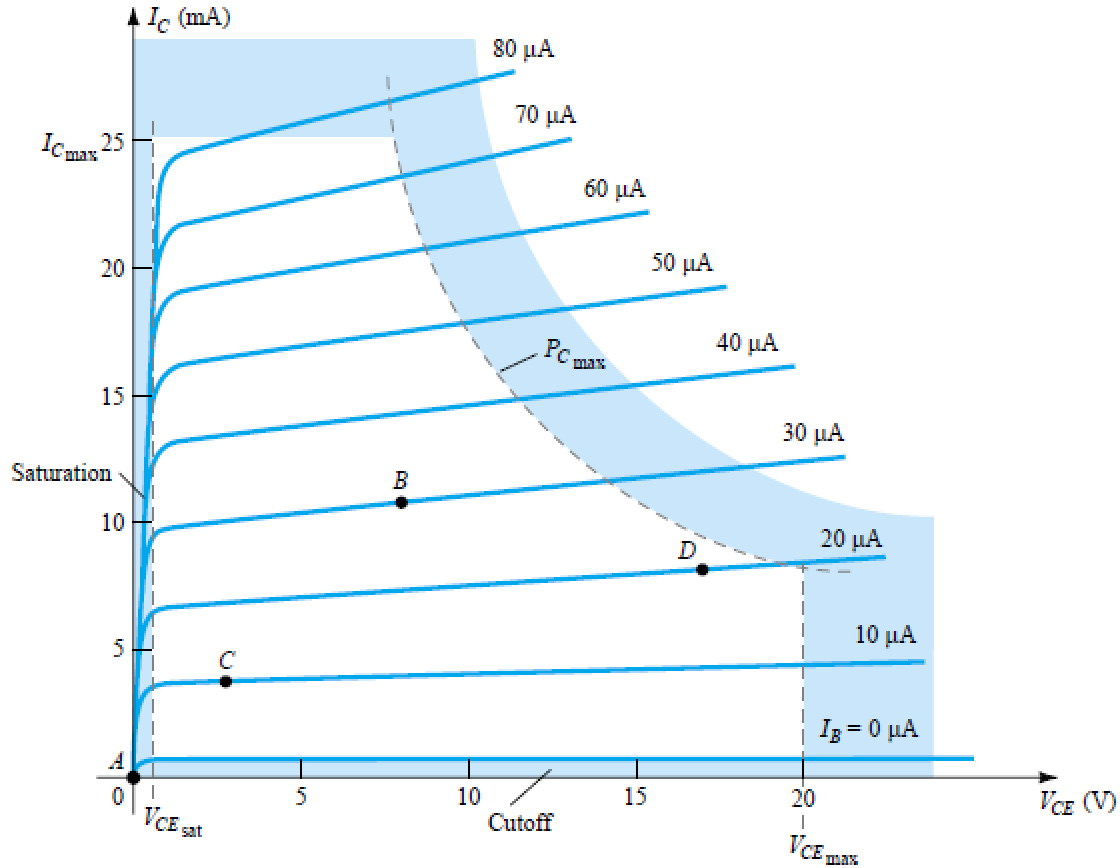
→ Compute performance of several important amplifier configurations.

→ Select an amplifier configuration appropriate for a given application.

Operating Point

- **Biasing:** The DC voltages applied to a transistor in order to turn it on so that it can amplify the AC signal.

- The DC input establishes an operating or quiescent point called the **Q-point**.



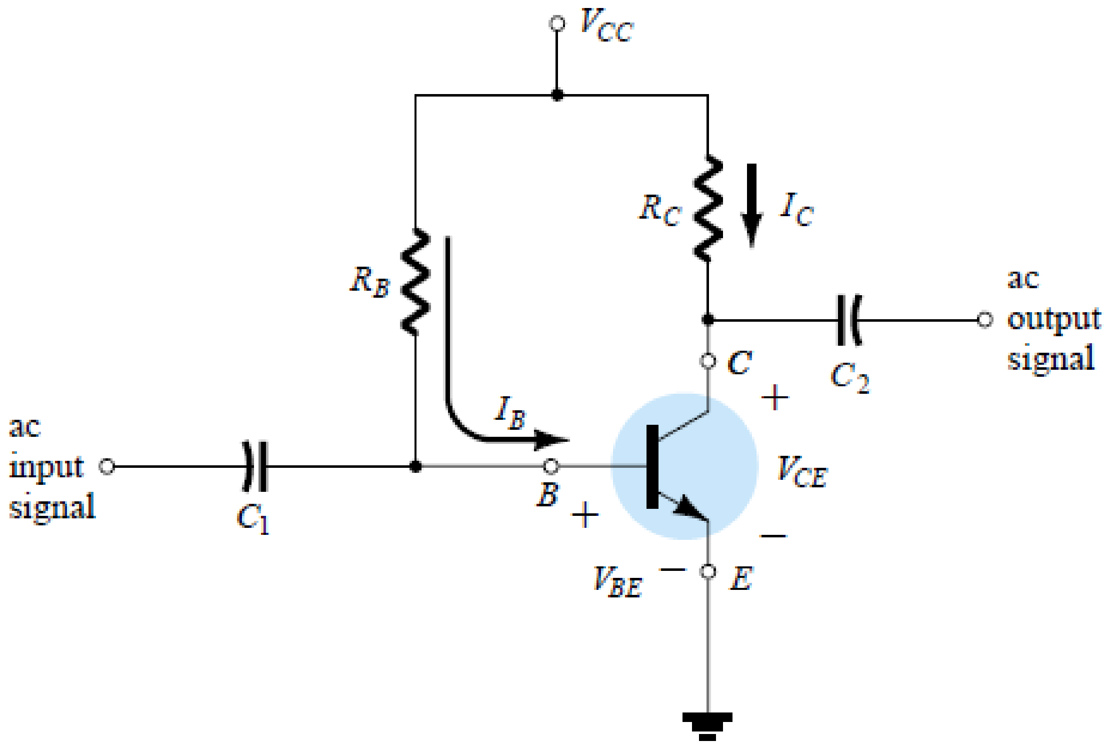
Operating Point

- **Active or Linear Region Operation**
  - Base–Emitter junction is forward biased
  - Base–Collector junction is reverse biased

- **Cutoff Region Operation**
  - Base–Emitter junction is reverse biased

- **Saturation Region Operation**
  - Base–Emitter junction is forward biased
  - Base–Collector junction is forward biased

Fixed-Bias Circuit



Fixed-Bias Circuit

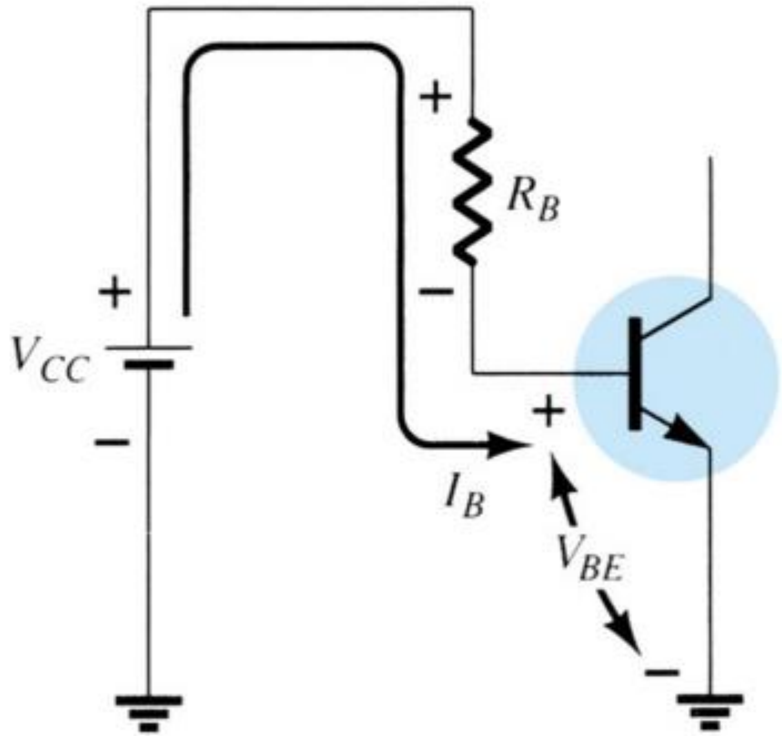
Base-Emitter Loop

- From Kirchhoff's voltage law:

$$+V_{CC} - I_B R_B - V_{BE} = 0$$

Solving for base current:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$



Fixed-Bias Circuit

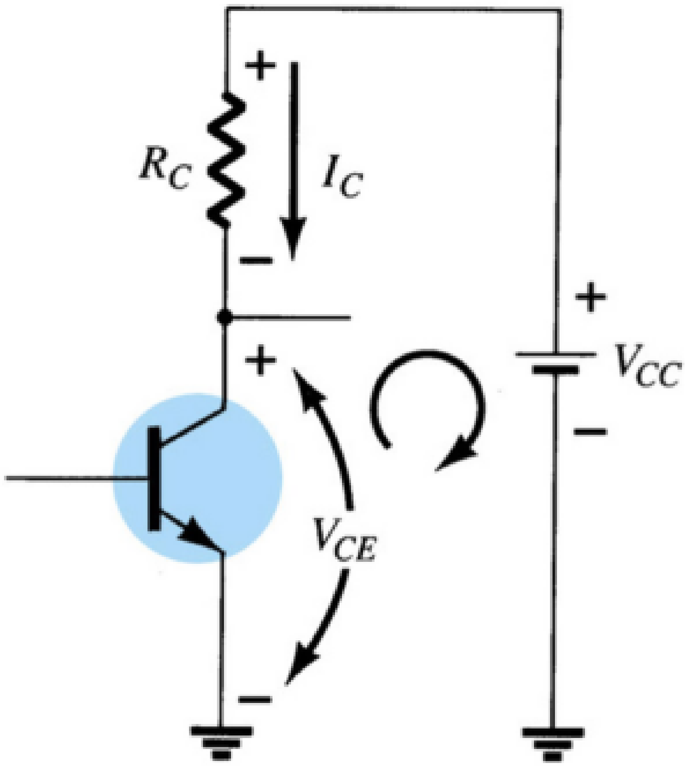
Collector-Emitter Loop

Collector current:

$$I_C = \beta I_B$$

- From Kirchhoff's voltage law:

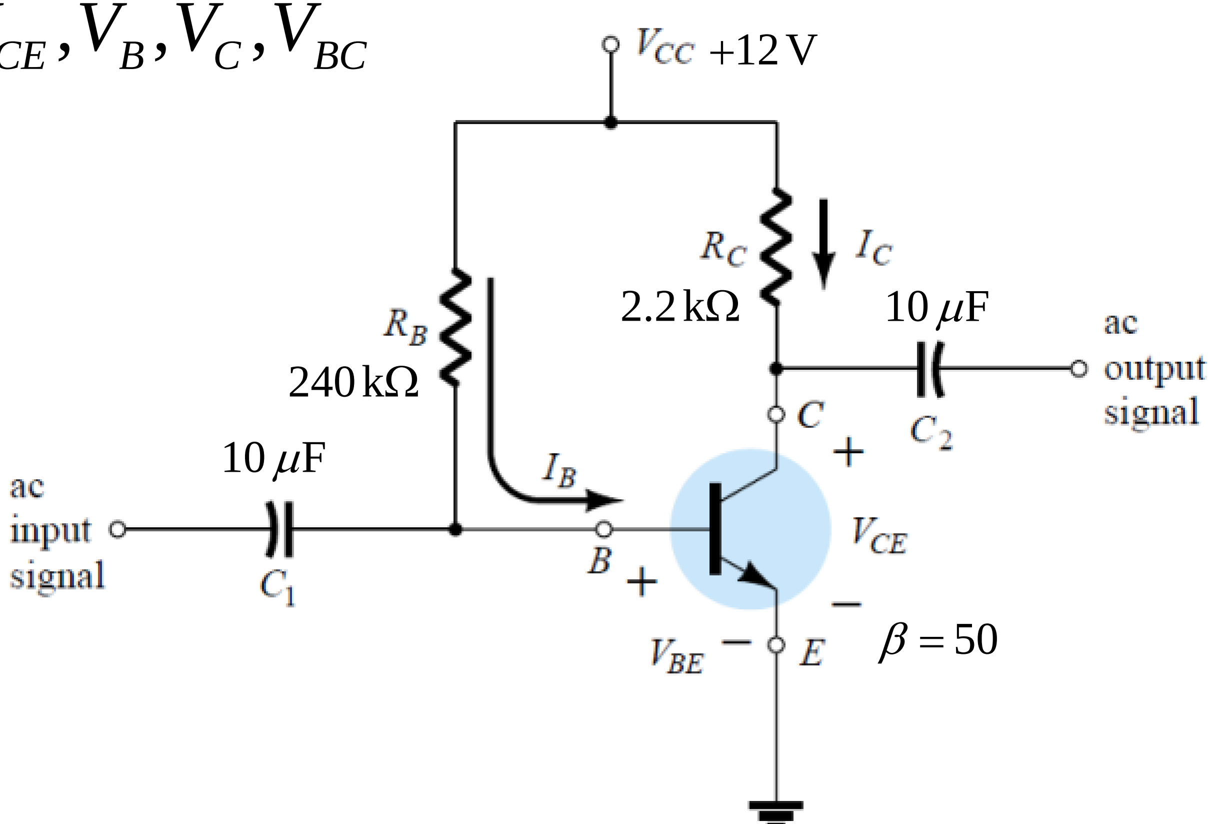
$$V_{CE} = V_{CC} - I_C R_C$$



Example 1

Determine the following for the fixed-bias configuration of figure shown

$$I_B, I_C, V_{CE}, V_B, V_C, V_{BC}$$



Example 1

Solution

Apply KVL to Base-Emitter loop,

$$-V_{CC} + R_B I_B + V_{BE} = 0$$

Then $$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$I_B = \frac{12 - 0.7}{240\,\text{k}} = 47.08\,\mu\text{A}$$

Collector current:

$$I_C = \beta I_B = 2.35\,\text{mA}$$

Apply KVL to Collector-Emitter loop,

$$V_{CE} = V_{CC} - I_C R_C$$

$$V_{CE} = 6.83\,\text{V}$$

$$V_B = V_{BE} = 0.7\,\text{V}$$

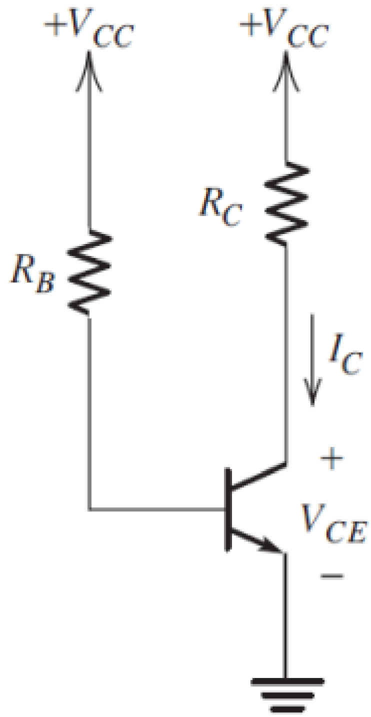
$$V_C = V_{CE} = 6.83\,\text{V}$$

$$V_{BC} = V_B - V_C$$

$$V_{BC} = -6.13\,\text{V}$$

Example 2

The dc bias circuit shown in figure below has $R_B = 200\ k\Omega$, $R_C = 1\ k\Omega$, and $V_{CC} = 15V$. The transistor β has = 100. Solve for I_C and V_{CE}



Example 2

Solution

Apply KVL to Base-Emitter loop,

$$-V_{CC} + R_B I_B + V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$I_B = \frac{15 - 0.7}{200\,\text{k}} = 71.5\,\mu\text{A}$$

Apply KVL to Collector-Emitter loop,

$$V_{CE} = V_{CC} - I_C R_C$$

$$V_{CE} = 15 - (7.15 \times 1\text{k}) = 7.85\,\text{V}$$

Collector current:

$$I_C = \beta I_B$$

$$I_C = (100)(71.5\mu)$$

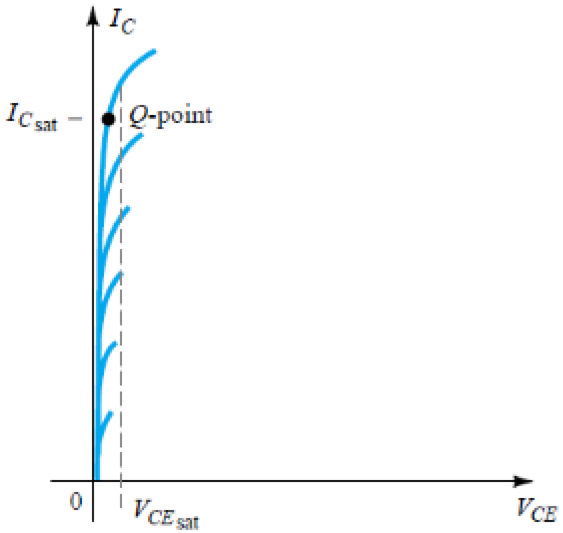
$$I_C = 7.15\,\text{mA}$$

Transistor Saturation

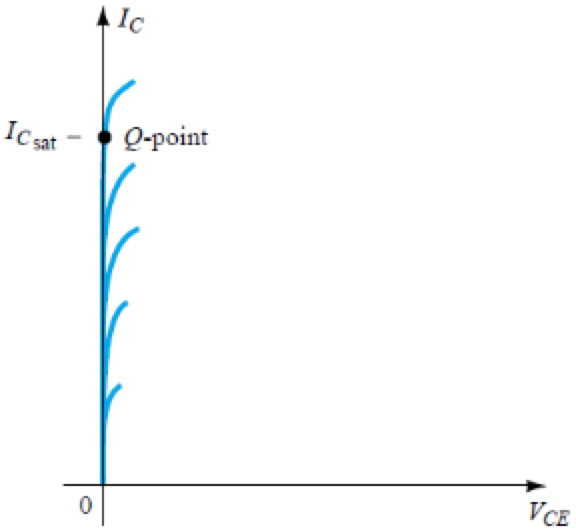
- When the transistor is operating in saturation, current through the transistor is at its maximum possible value.

$$I_{C_{sat}} = \frac{V_{CC}}{R_C}$$

$$V_{CE} \cong 0\ \text{V}$$



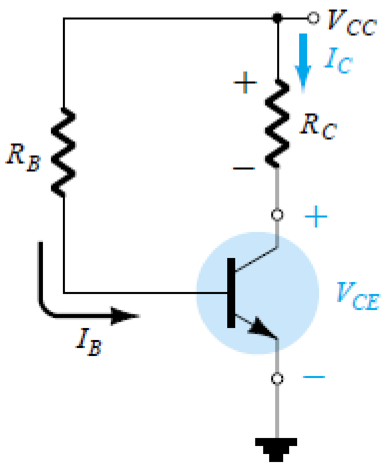
Actual

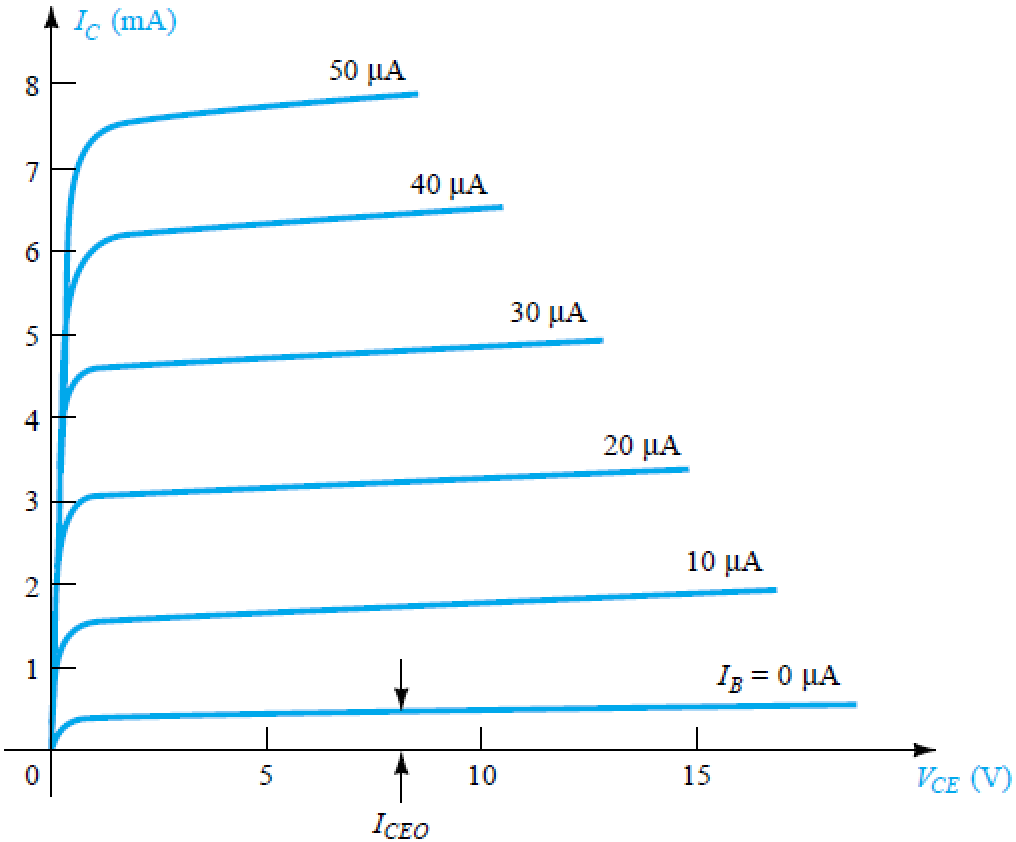


Approximate

Fixed-Bias Circuit

Load-Line Analysis





I Mohd-Khairuddin , Z Md-Yusof

Load-Line Analysis

- The end points of the load line are:

I_{Csat}

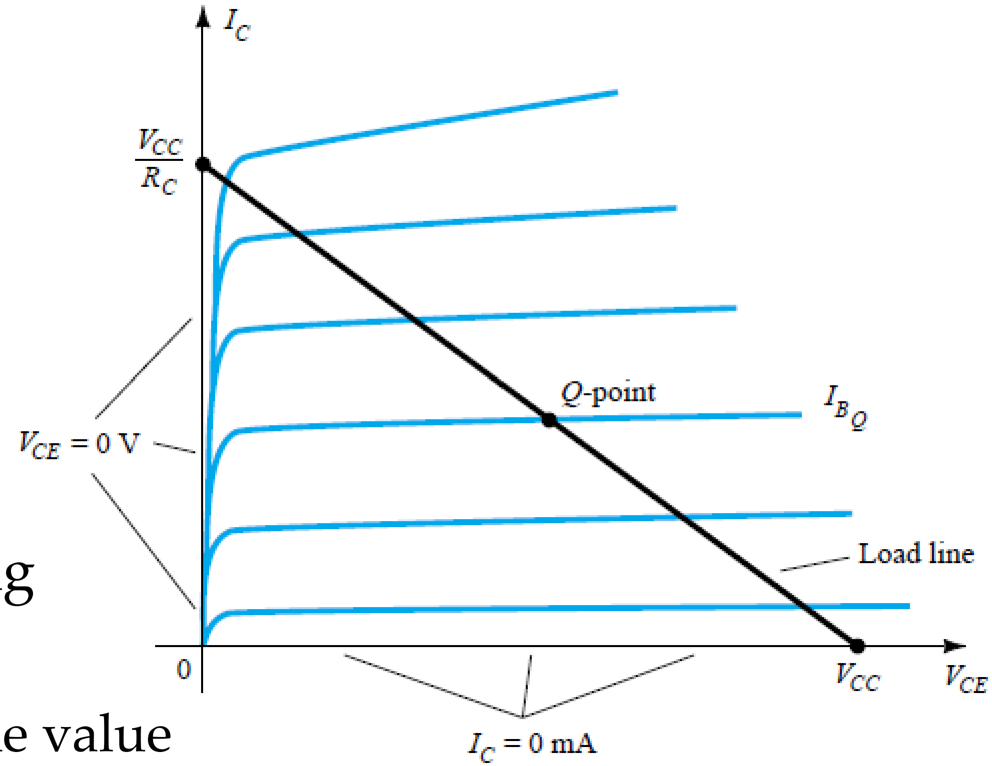
$I_C = V_{CC} / R_C$

$V_{CE} = 0$ V

$V_{CEcutoff}$

$V_{CE} = V_{CC}$

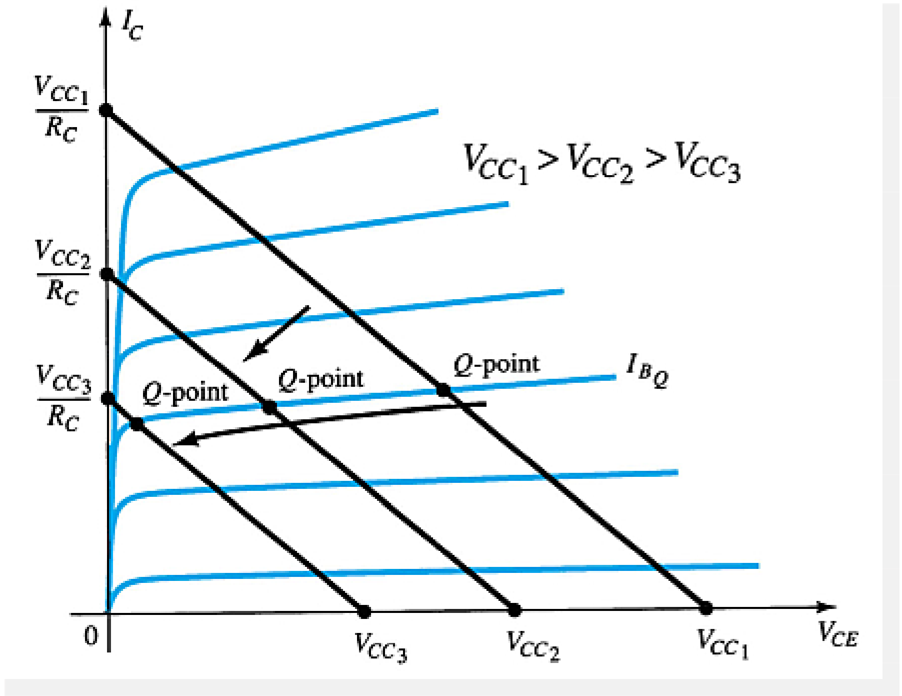
$I_C = 0$ mA

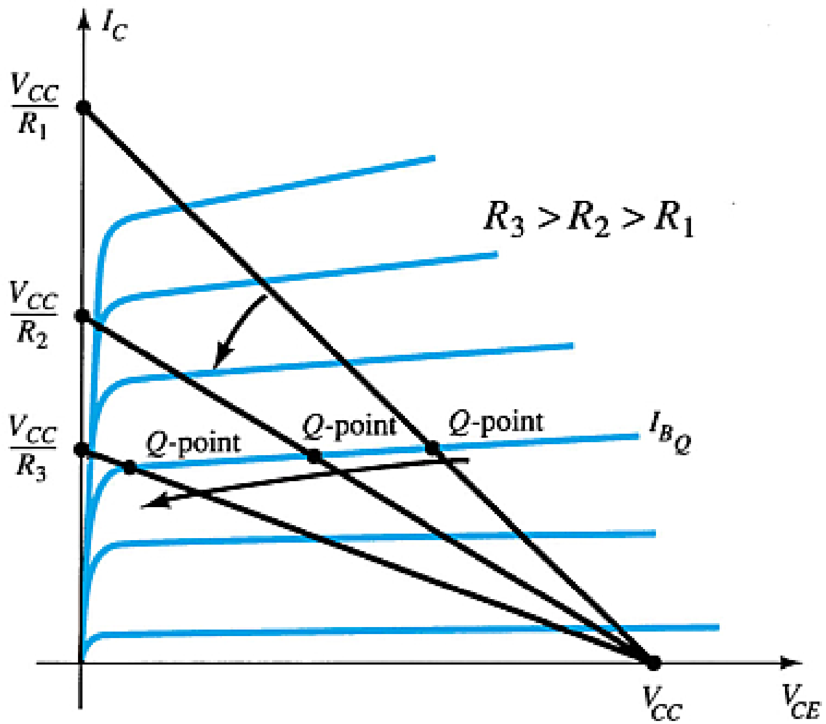


- The *Q*-point is the operating point:
  - where the value of R_B sets the value of I_B
  - that sets the values of V_{CE} and I_C

Fixed-Bias Circuit

Circuit Values Affect the Q-Point





Circuit Values Affect the Q-Point

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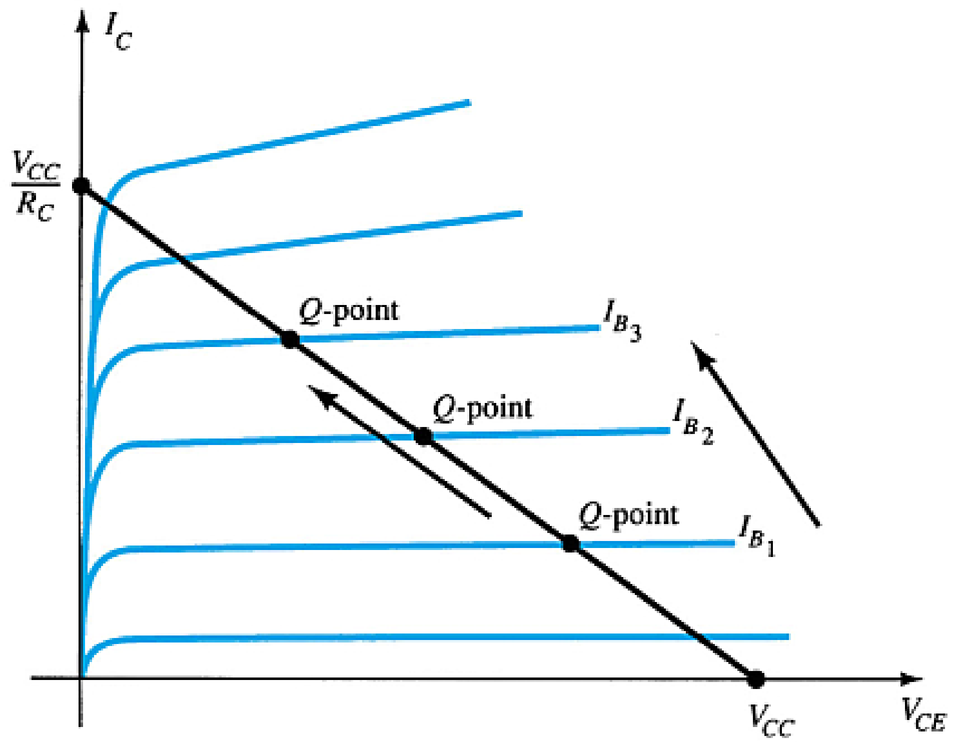
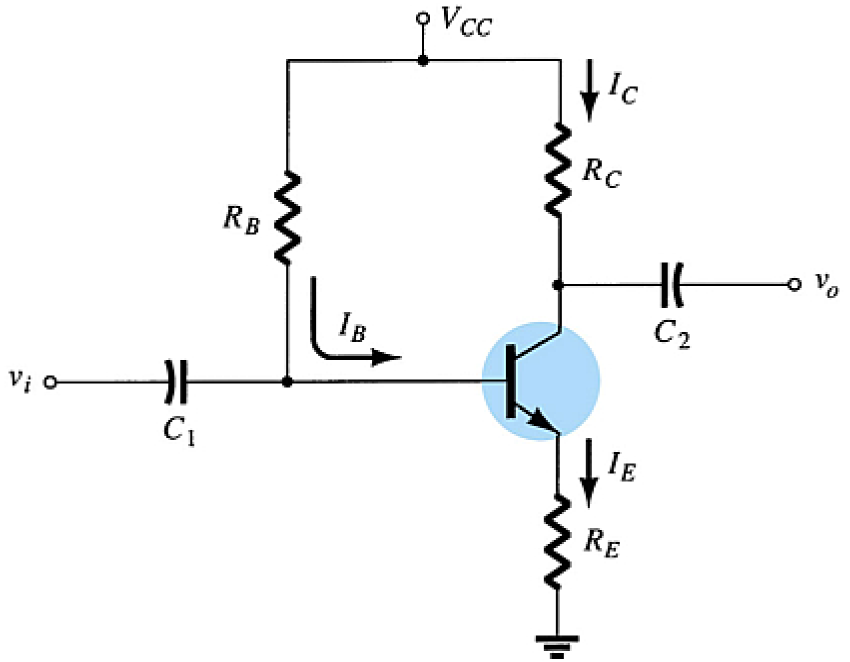


Emitter Bias

- Adding a resistor (R_E) to the emitter circuit stabilizes the bias circuit.



Base-Emitter Loop

- From Kirchhoff's voltage law:

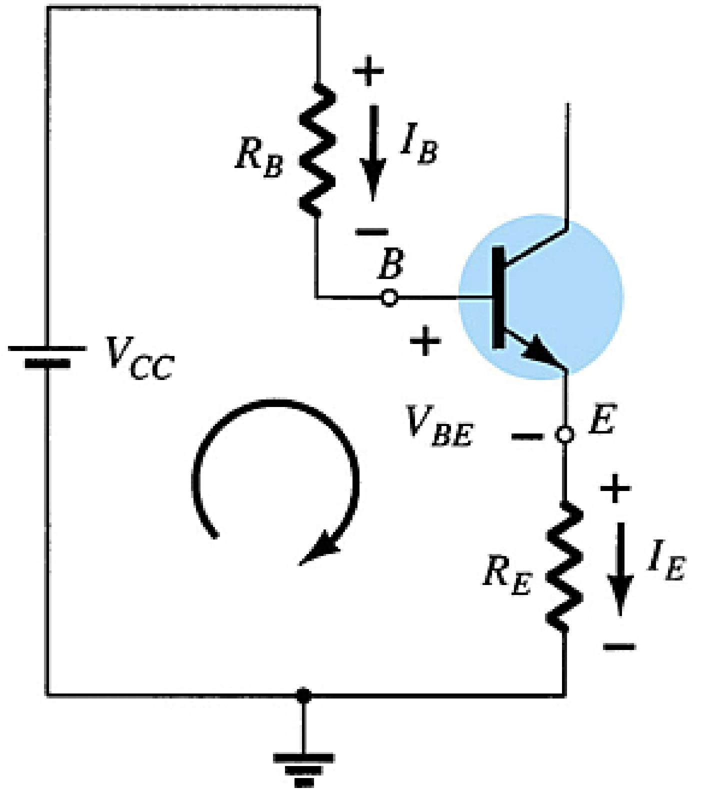
$$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

- Since $I_E = (\beta + 1)I_B$:

$$V_{CC} - I_B R_B - (\beta + 1) I_B R_E = 0$$

- Solving for I_B:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E}$$



Collector-Emitter Loop

- From Kirchhoff's voltage law:

$$I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

- Since $I_E \cong I_C$:

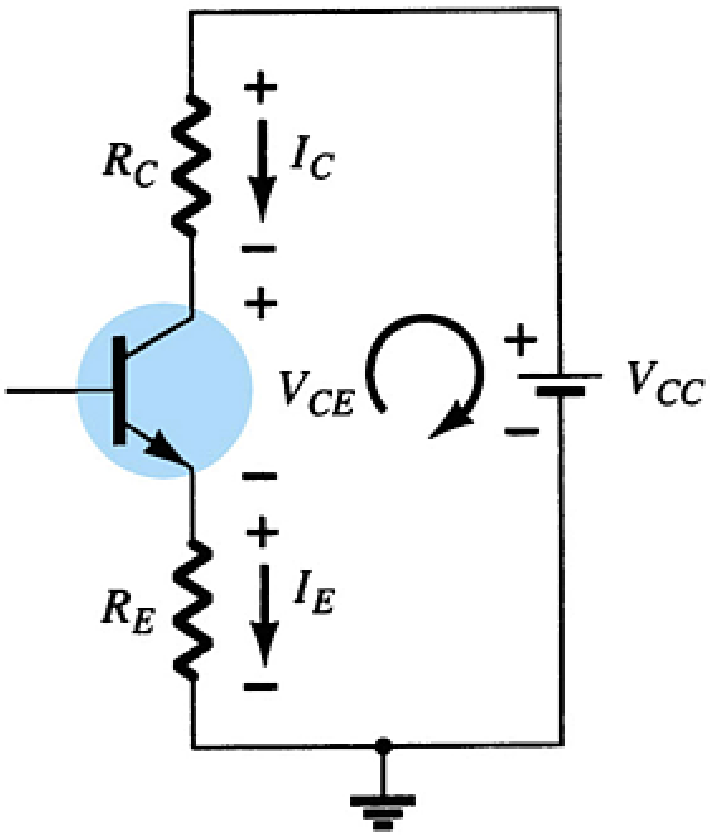
$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

- Also:

$$V_E = I_E R_E$$

$$V_C = V_{CE} + V_E = V_{CC} - I_C R_C$$

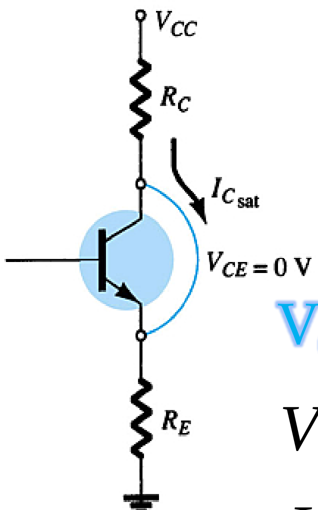
$$V_B = V_{CC} - I_R R_B = V_{BE} + V_E$$



Improved Biased Stability

- Stability refers to a circuit condition in which the currents and voltages will remain fairly constant over a wide range of temperatures and transistor Beta (β) values.
- Adding R_E to the emitter improves the stability of a transistor.

Saturation Level



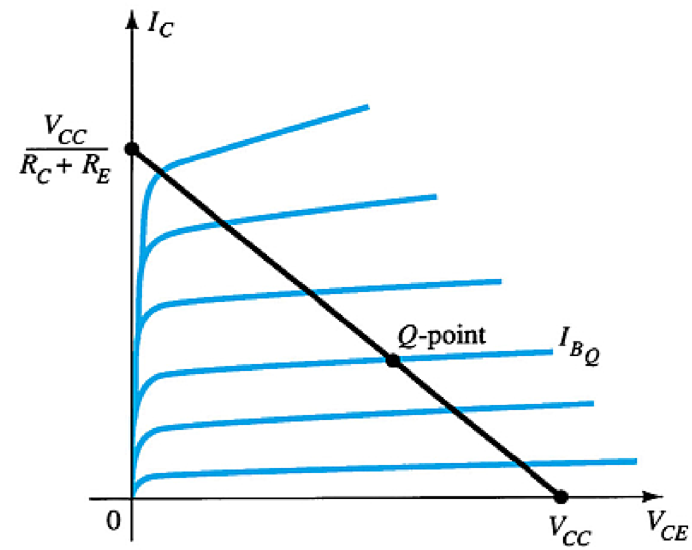
- The endpoints can be determined from the load line.

$V_{CEcutoff}$:

$$V_{CE} = V_{CC}$$
$$I_C = 0 \text{ mA}$$

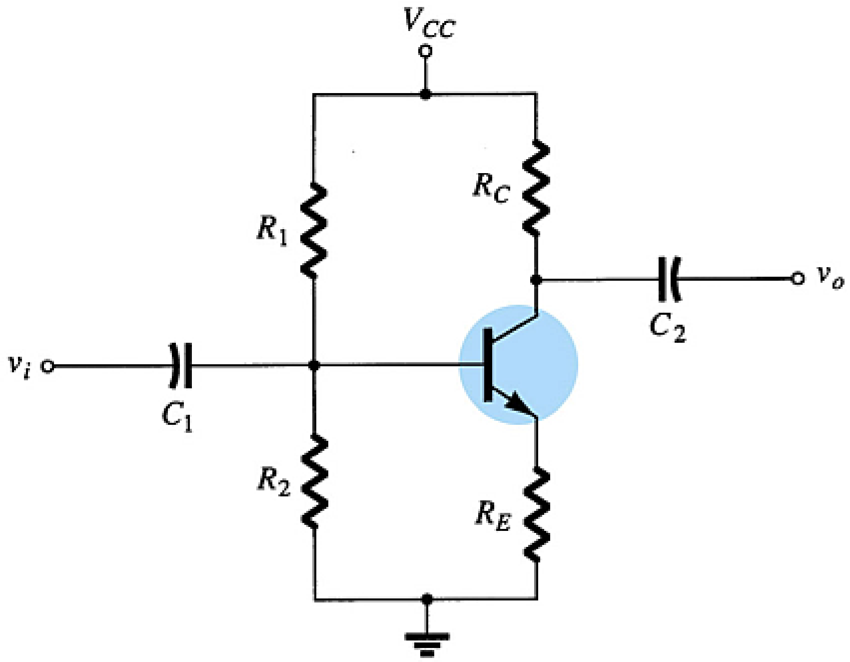
I_{Csat}:

$$V_{CE} = 0 \text{ V}$$
$$I_C = \frac{V_{CC}}{R_C + R_E}$$



Voltage Divider Bias

- This is a very stable bias circuit.
- The currents and voltages are nearly independent of any variations in β.



Approximate Analysis

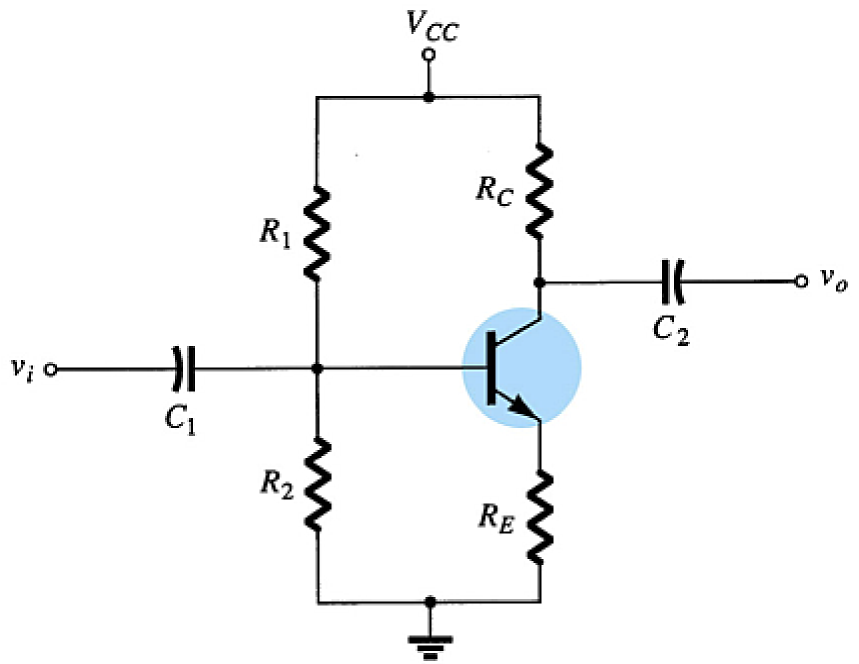
- Where $I_B << I_1$ and $I_1 \cong I_2$:

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2}$$

- Where $\beta R_E > 10R_2$:

$$I_E = \frac{V_E}{R_E}$$

$$V_E = V_B - V_{BE}$$



- From Kirchhoff's voltage law:

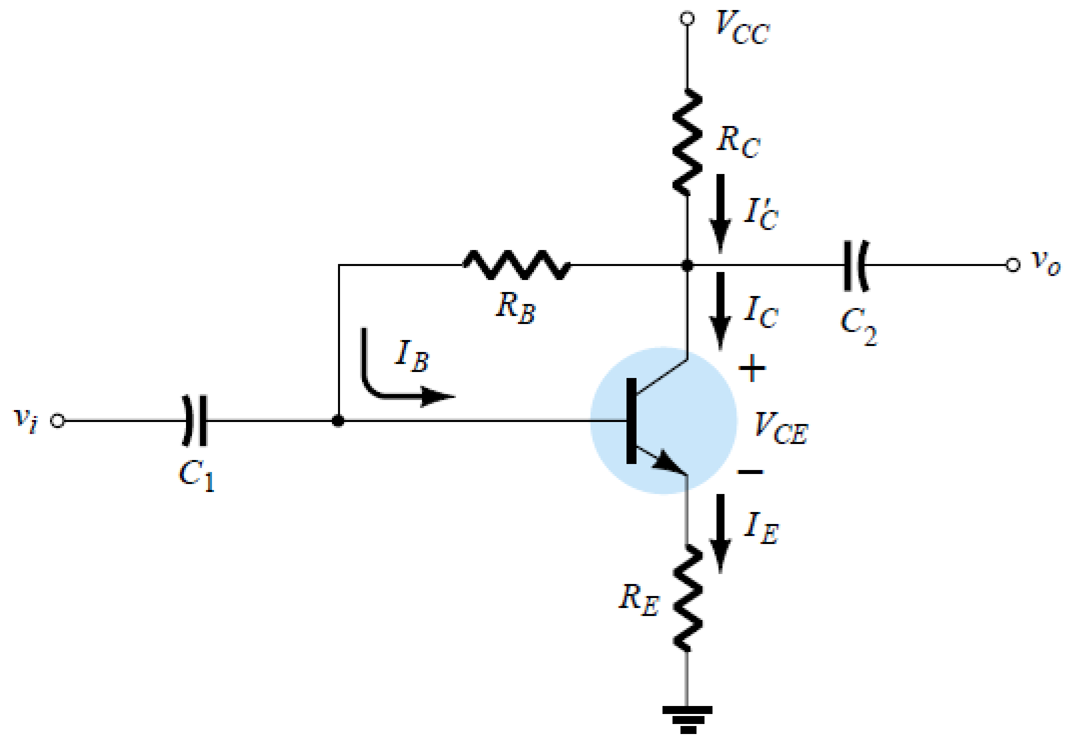
$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$I_E \cong I_C$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

DC Bias With Voltage Feedback

- Another way to improve the stability of a bias circuit is to add a feedback path from collector to base.
- In this bias circuit the Q-point is only slightly dependent on the transistor beta, β.



Base-Emitter Loop

- From Kirchhoff's voltage law:

$$V_{CC} - I_C^{'}R_C - I_B R_B - V_{BE} - I_E R_E = 0$$

- Where $I_B << I_C$:

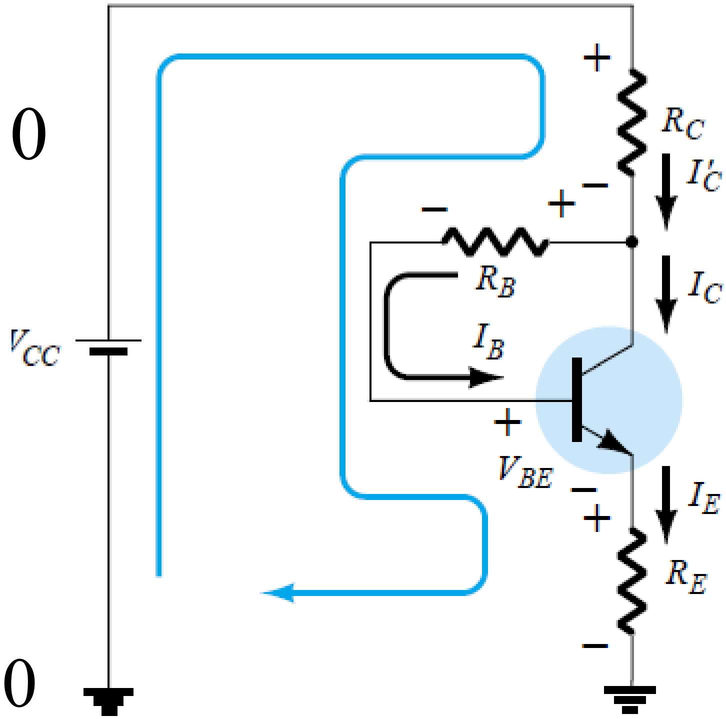
$$I_C^{'} = I_C + I_B \cong I_C$$

- Knowing $I_C = \beta I_B$ and $I_E \cong I_C$, the loop equation becomes:

$$V_{CC} - \beta I_B R_C - I_B R_B - V_{BE} - \beta I_B R_E = 0$$

- Solving for I_B:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}$$



Design Operations

Base-Emitter Bias Analysis

Transistor Saturation Level

$$I_{Csat} = I_{Cmax} = \frac{V_{CC}}{R_C + R_E}$$

Load Line Analysis

Cutoff:

$$V_{CE} = V_{CC}$$
$$I_C = 0\,mA$$

Saturation:

$$I_C = \frac{V_{CC}}{R_C + R_E}$$
$$V_{CE} = 0\,V$$

PNP Transistor

- The analysis for *pnp* transistor biasing circuits is the same as that for *npn* transistor circuits. The only difference is that the currents are flowing in the opposite direction.