Faculty of Electrical & Electronics Engineering
BEE1213 DIGITAL ELECTRONICS

LAB 2: COUNTER DESIGN

Mapping CO,PO,Domain,KI : CO4, PO5
CO4: Construct logic circuit and counter PO5: Create, select and apply appropriate techniques, resources, and modern engineering and IT tools, including prediction and modelling, to complex engineering activities, with an understanding of the limitations.

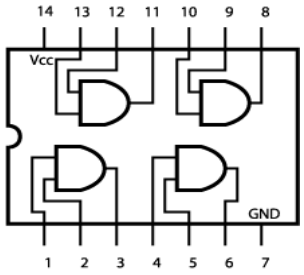
Learning Outcomes

At the end of the experiment, student should be able to:
• implement flip flops in designing counter.
• design and construct a synchronous counter.

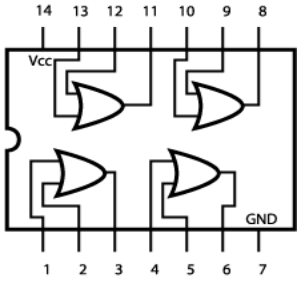
Technical Notes

This is the introductory laboratory session, to allow you to become familiar with very basic digital circuits and the equipment that you will use for the remainder of the experiments.

Useful IC Diagrams:

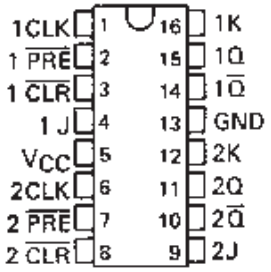


7408(AND)



7432(OR)

SN5476, SN54LS76A . . . J PACKAGE
SN7476 . . . N PACKAGE
SN74LS76A . . . D OR N PACKAGE
(TOP VIEW)



Equipment needed:

- Digital Trainer
- 7408 2-input AND
- 7432 2-input OR
- 7476/5476 - JK Flip-flop with preset & clear

Project Task:

Task 1: Synchronous Counter (Theory)

- Theoretically design a 3-bit synchronous counter with the sequence below by using JK flip flops.

$$1 \rightarrow 5 \rightarrow 3 \rightarrow 7 \rightarrow 4 \rightarrow 0 \rightarrow 2 \rightarrow 6 \rightarrow ...$$

- Show all steps in your design (state diagram, excitation table, K-map, circuit drawing) by completing the worksheet given.

Task2: Synchronous Counter (Software simulation)

- Design a 3-bit synchronous counter with the sequence below by using JK flip flops.

$$1 \rightarrow 5 \rightarrow 3 \rightarrow 7 \rightarrow 4 \rightarrow 0 \rightarrow 2 \rightarrow 6 \rightarrow ...$$

- Apply the clock pulses and observe the output.
- Verify your design with output waveform simulation.
- Attach the schematic and output waveform printout with worksheet in Task 1.

Task2: Synchronous Counter (Hardware)

- Construct a 3-bit synchronous counter with the sequence below by using JK flip flops and basic logic gate IC chips.

$$1 \rightarrow 5 \rightarrow 3 \rightarrow 7 \rightarrow 4 \rightarrow 0 \rightarrow 2 \rightarrow 6 \rightarrow ...$$

- Tabulate the output logic and compare results with theoretical answers.

Familiarize yourself with each IC by using their data sheets. You will be assessed based on all three parts of the lab: theoretical, simulation and hardware. A Q&A session will be done to test your understanding of what you're doing.

APPENDIX: LAB 2 WORKSHEET

Instruction: Design a 3-bit synchronous counter with the sequence below by using JK flip flops.

1→ 5 → 3 → 7 → 4→ 0→ 2 → 6 → ...

Design your counter before entering lab session and submit at the end of lab session.

TASK 1

1. State diagram:

2. Excitation table:

3. K-map:

4. Circuit implementation:

TASK 3

Compare results with theoretical answers.

Clock	Counting sequence (Theory)	Counting sequence (Practical)
	001	
	101	
	011	
	111	
	100	
	000	
	010	
	110	
	000 (repeat)	