Tutorial 2
Chapter 3: Logic Gates & Boolean Algebra
&
Chapter 4: Cobinational Logic Circuit

Test 1 Sem I 2010/2011

1. Figure 1 shows a combinational logic circuit.

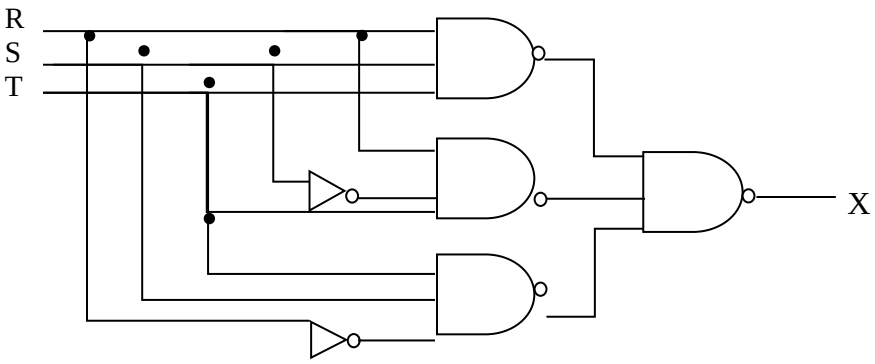

Figure 1

(i) Find expression X

Test 2 Sem I 2010/2011

2. (a) Define *fan-out*
   (b) Figure 2 shows the DC noise margins. Explain indeterminate range.
   (c) The input/output voltage specifications for the standard TTL family are list in Table 1. Use these values to determine the following for 74AS IC:
      (i) High-state noise margin, V_{NH}
      (ii) Low-state noise margin, V_{NL}

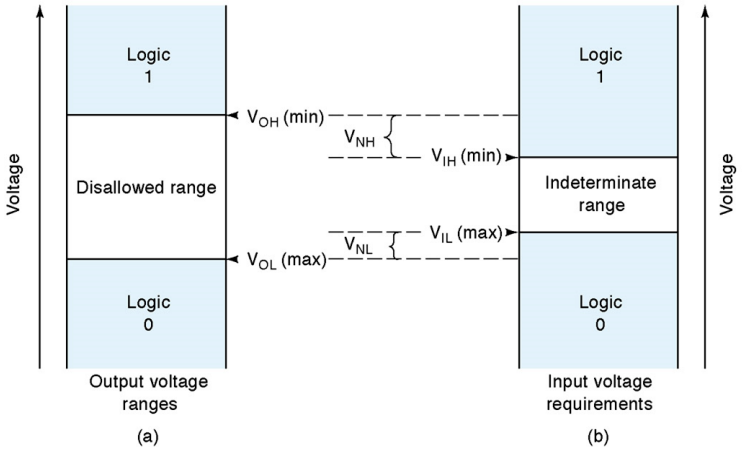

Figure 2

Table 1: Typical TTL series characteristics

	74	74S	74LS	74AS	74ALS	74F
Performance ratings:						
Propagation Delay (ns)	9	3	9.5	1.7	4	3
Power dissipation (mW)	10	20	2	8	1.2	6
Max clock rate (MHz)	35	125	45	200	70	100
Fan-out (same series)	10	20	20	40	20	33
Voltage parameters:						
V_{OH} (min) (V)	2.4	2.7	2.7	2.5	2.5	2.5
V_{OL} (max) (V)	0.4	0.5	0.5	0.5	0.5	0.5
V_{IH} (min) (V)	2	2	2	2	2	2
V_{IL} (max) (V)	0.8	0.8	0.8	0.8	0.8	0.8

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3. Regarding to the logic circuit as shown in Figure 3:
   (a) Simplify a Boolean expression
   $\overline{A\bar{B}}(\bar{A}+B)(\bar{B}+B)$
   (b) Regarding to the combinational logic circuit as shown in Figure 3

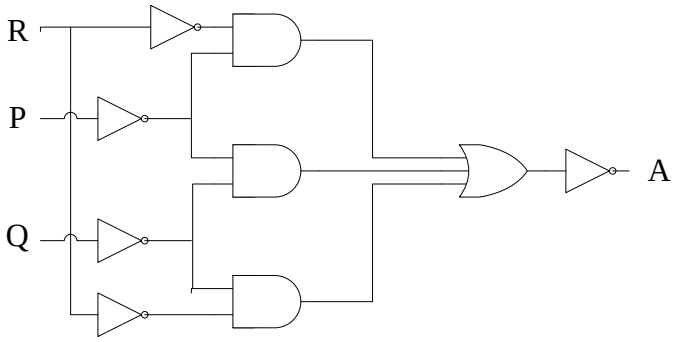

Figure 3

(i) Find the expression of A
(ii) Simplify A
(iii) Draw the simplified circuit
(iv) Redraw the simplified circuit by using only NOR gate

[10 Marks]

4. In designing a combinational circuit, there are two methods available to acquire the most simplified logic circuit. Given the Boolean function, do the following:

$$f(A,B,C)=\sum_{m}(0,1,3,5,7)$$

(i) Derive the truth table and SOP expression for the system
(ii) Use algebraic simplification to simplify the expression x_1 acquired in (b) and draw its logic circuit diagram
(iii) Use k-maps to get the simplified expression x_2 and draw its circuit diagram
(iv) Compare the two methods of simplification

[13 Marks]

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5. (a) Convert the following Boolean expression into standard Product-of-Sum (POS) form:

$$(A+B+\overline{C})(\overline{B}+D)(\overline{A}+B+C+\overline{D})$$

$$Ans=(A+\overline{B}+\overline{C}+D)(A+\overline{B}+\overline{C}+\overline{D})(A+\overline{B}+C+D)(A+\overline{B}+\overline{C}+D)(\overline{A}+\overline{B}+C+D)(\overline{A}+\overline{B}+\overline{C}+D)(A+\overline{B}+\overline{C}+D)$$

[4 Marks]

(b) In designing a combinational circuit, there are two methods available to acquire the most simplified logic circuit. Given the Boolean function, do the following:

$$X=f(A,B,C)=\sum_m(0,2,3,6,7)$$

(i) Derive the truth table and SOP expression from **X**. (Ans: $X=\overline{A}\overline{B}\overline{C}+\overline{A}B\overline{C}+\overline{A}BC+AB\overline{C}+ABC$)
(ii) Use algebraic simplification to simplify the expression acquired in (a). (Ans: $X=\overline{A}\overline{B}\overline{C}+B$ or $X=\overline{A}\overline{C}+B$)
(iii) Use k-maps to simplify the expression acquired in (a). (Ans: $X=\overline{A}\overline{C}+B$)
(iv) Implement the simplified expression in (c) in circuit diagram.
(v) Redraw the simplified circuit by using only NOR gate.

[16 Marks]

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6. Two different logic circuits have the characteristics shown in Table 2.
(i) Which circuit has the best LOW- state dc noise immunity?
(ii) Which circuit has the best HIGH-state dc noise immunity?

[4 Marks]

Table 2

	Circuit A	Circuit B
V_{supply}	6	5
V_{IH}(min) (V)	1.5	1.7
V_{IL}(max) (V)	0.6	0.9
V_{OH}(min) (V)	2.4	2.5

V_{OL}(max) (V)	0.5	0.4
t_{PLH}(ns)	10	28
t_{PHL}(ns)	8	14
P_D (mW)	16	10

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7. (a) In one digital system an *odd-parity* bit is included at the end of the code. This system using BCD code to represent the decimal numbers from 000 to 999. Determine whether the code groups below have an error or not, the code has been transferred from one location to another.
   (i) 1001010110000
   (ii) 0100011101100
   (iii) 0111101000011

[6 Marks]

(b) In Pineapple Auto Sdn. Bhd., they are using automatic system to sorting the grade of pineapple fruit. In that system, the conveyor belt will shut down whenever specific conditions occur. These conditions are monitored and reflected by the states of four logic signals as follows:

Signal A = HIGH; when conveyer belt speed is too fast
Signal B = HIGH; when the collection bin at the end of the conveyer is full
Signal C = HIGH; when the belt tension is too high
Signal D = HIGH; when manual override is off

(i) Generate a logic circuit to off the operation of the conveyor belt. The conveyor will be stop whenever conditions A and B exist simultaneously or whenever conditions C and D exist simultaneously.
(ii) Implement the circuit in (i) using NAND gate
(iii) Comment your answer in (ii) if we implement both circuits using IC in **Appendix A.**

[10 Marks]

(c) Design a circuit that produces a HIGH out only when all three inputs are the same level.
(i) Draw the truth table and express the equation in Sum-of-product (SOP).
(ii) Simplified the circuit using Karnaugh-Map.
(iii) Implement the simplified circuit using 2-input exclusive-or gate and other suitable gates.

[9 Marks]

8. (a) Fan-out is a maximum number of standard logic inputs that the output of a digital circuit can reliably drive. Refer to the datasheet in **Appendix B**, determine how many AND gates input can be driven by the output of another AND gate.

[6 Marks]

(b) Compute the High level and Low level noise margins for 3.3 V CMOS by using the information in Figure 4.

[5 Marks]

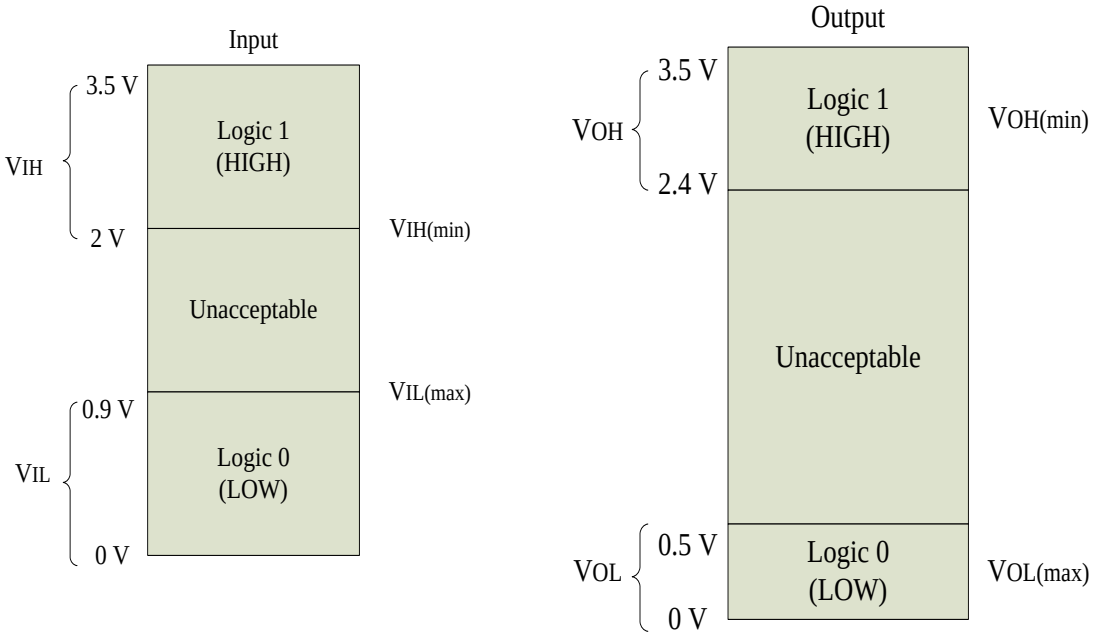

Figure 4

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9. (a) Apply DeMorgan's theorem to the expression $\overline{(\bar{A}+B)+CD}$ and draw the last expression using only NAND and OR gates.

[5 Marks]

(b) Given are the sets of Boolean function:

$$f_1(a,b,c,) = \sum_m (1,3,5,6,7)$$
$$f_2(a,b,c,) = \sum_m (1,3,4,6)$$
$$f_1(a,b,c,) = \sum_m (0,2,4,5,7)$$

Simplify all those Boolean functions by using Karnaugh map method

[14 Marks]

10. (a) Simplify $Z = \bar{A}C(\overline{\bar{A}BD}) + \bar{A}B\bar{C}\bar{D} + A\bar{B}C$ using algebraic simplification. Then use Karnaugh map to prove that this equation can be simplified further than the answer from algebraic simplification.

[16 Marks]

(b) The input/output voltage specifications for the standard TTL family are list in Table 3. Use these values to determine:

(i) V_{NH}

(ii) V_{NL}

[4 Marks]

Table 3

Parameter	Min (V)	Typical (V)	Max (V)
V_{OH}	2.4	3.4	-
V_{OL}	-	0.2	0.4
V_{IH}	2	-	-
V_{IL}	-	-	0.8

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11. $X = \overline{AB + AC} + A\bar{B}C$

(i) Use algebraic simplification to simplify X

(ii) Implement the simplified expression in (i) in circuit diagram

(iii) Use Karnaugh Map method to simplify X

(iv) Redraw the simplified circuit by using only NAND gate.

[14 Marks]

12. Find the expression x and simplify using Boolean Algebra Theorems of circuit in Figure 5.

[6 Marks]

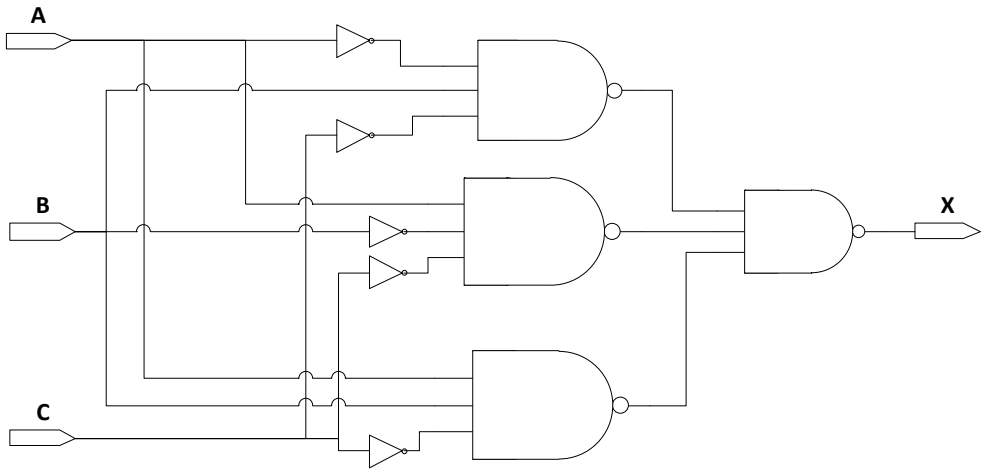

Figure 5

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13. Given a combinational logic gates as shown in Figure 6

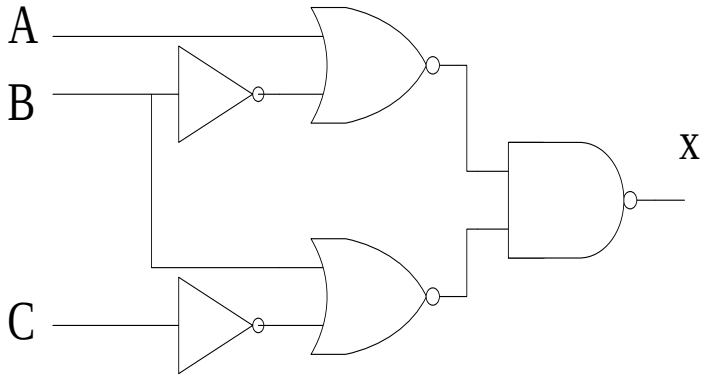


Figure 6

(i) Write the expression for X

(ii) Derive the truth table for X

(iii) Simplify X

(iv) Apply the waveform in Figure 7 to the inputs, and then draw the resulting output waveform.

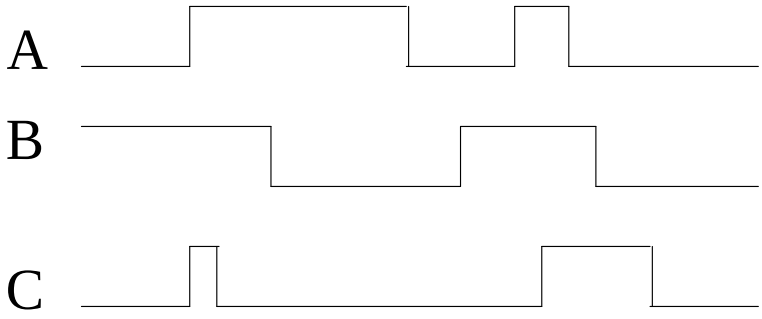


Figure 7

[7 Marks]

14. (i) Convert the following Boolean expression into standard POS

$$(\bar{A} + B + \bar{C})(\bar{B} + \bar{C} + D)(A + B + \bar{C} + \bar{D})$$

(ii) Convert the SOP expression to an equivalent POS expression

$$ABC + \bar{A}B\bar{C} + A\bar{B}C + A\bar{B}\bar{C}$$

[4 Marks]

15. Given are the sets of Boolean function:

$$f_1(P, Q, R, S) = \sum_m (0,4,5,8,10,12,14)$$

$$f_2(P, Q, R, S) = \sum_m (2,3,4,5,9,10,13)$$

(i) Produce the logic equations for f_1 and f_2 in SOP form.

(ii) Use Karnaugh map method for minimization and obtain the minimized expressions.

(iii) Draw both logic circuits for the minimize expressions.

[17 Marks]

16. Table 4 shows the list of input to the parity checker in Figure 8. Find the output of the parity checker in Figure 8 for each of the following sets of data from the transmitter.

Table 4: Data sets from the transmitter

	P	D_3	D_2	D_1	D_0
(i)	0	1	1	0	1
(ii)	0	0	1	1	1
(iii)	1	1	0	0	0
(iv)	1	1	1	1	1

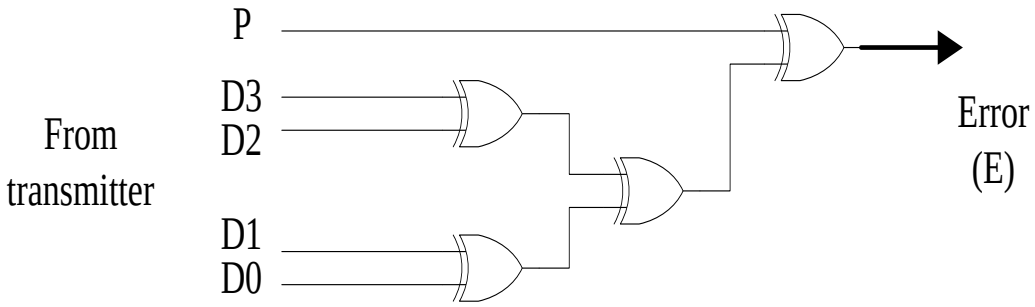
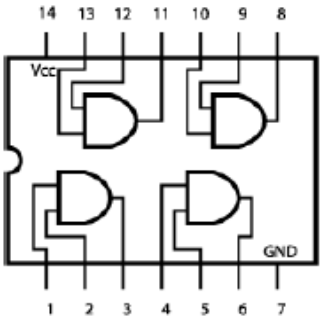


Figure 6

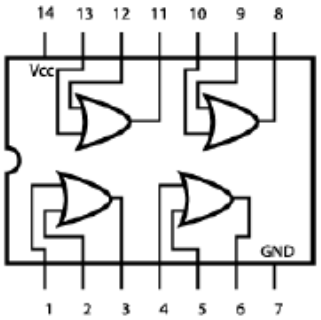
[4 marks]

APPENDIXA

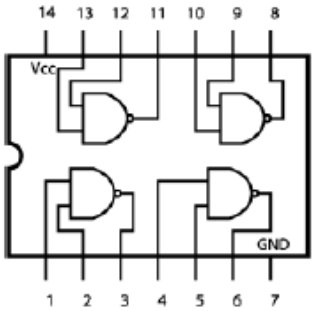
IC DIAGRAMS



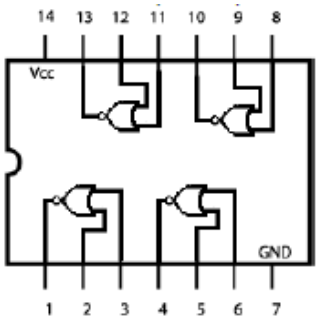
7408(AND)



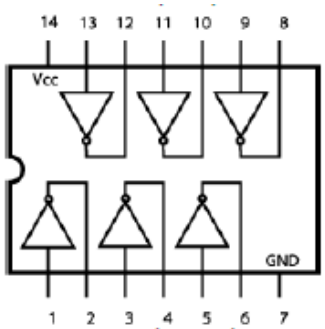
7432(OR)



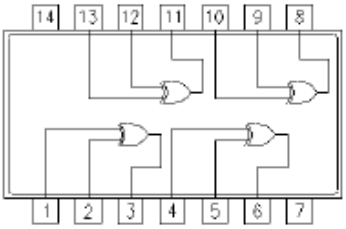
7400(NAND)



7402(NOR)



7404(NOT)



7486 (XOR)

APPENDIX B

Quad 2-input AND gate | 74ALS08

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	16	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–0.4	mA
I_{OL}	Low-level output current			8	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC}±10%, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = –0.4mA		V_{CC} – 2			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 4mA		0.25	0.40	V
				I_{OL} = 8mA		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.1	mA
I_O	Output current[3]		V_{CC} = MAX, V_O = 2.25V		-30		-112	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_I = 4.5V		1.3	2.4	mA
		I_{CCL}		V_I = 0V		2.2	4.0	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. The output conditions have been chosen to produce a current that closely approximate one half of the true short-circuit output current, I_{OS}.